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	[3]	SOC: VIDEO														
	[4]	SOC: POWER: MEMIO,CPUCORE,NBCORE,MISC														
	[5]	SOC: POWER: V_GFXCORE														
	[6]	SOC: POWER: VSS														
	[7]	SOC: POWER: VSS														
	[8]	SOC: MEMORY PARTITION F1 & F0														
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	[16]	SOC: DECOUPLING														
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	[31]	MEMORY: CHANNEL F1														
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	[34]	KIC: USB														
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[40]	KIC: POWER															
[41]	KIC: DECOUPLING															
[42]	ETHERNET CONTROLLER															
[43]	EMMC MEMORY															
[44]	CONN: RJ45,TOSLINK															
[45]	CONN: USB (FRONT & REAR)															
[46]	CONN: WIFI															
[47]	CONN: HDMI IN															
[48]	CONN: HDMI OUT															
[49]	HDMI LOAD SWITCHES															
[50]	CONN: ODD & HDD															
[51]	CONN: FRONT PANEL, FAN, AUDIO															
[52]	CONN: POWER															
[53]	VREGS: INPUT FILTERS															
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[58]	VREGS: MEMIO & MEMPHY															
[59]	VREGS: MEMPHY OUTPUT															
[60]	VREGS: MEMIO OUTPUT															
[61]	VREGS: NBCORE															
[62]	VREGS: V5P0															
[63]	VREGS: V3P3, VSOC1P8															
[64]	VREGS: VSOCPHY/VFUSE															
[65]	VREGS: V_SB1P8, V_SB1P1															
[66]	VREGS: V3P3 STANDBY															
[67]	VREGS: V1P1 STANDBY, V1P8 STANDBY															
[68]	STANDBY GATES															
[69]	IR BLASTER															
[70]	I2C															
[71]	MARGIN: SOCPHY,SOC1P8,MEMIO,NBCORE															
[72]	MONITOR: VSOC1P8, VSOCPHY, V12P0															
[73]	CONN: FACET BOARD															
[74]	CONN: SWITCHES															
[75]	CONN: HDT															
[76]	CONN: M.2															
[77]	CLOCK BUFFER															
[78]	PREMIUM SPEAKER (SE/LE)															
[79]	DEBUG: VR HEADERS, TEST POINTS, CONNECTORS															
[80]	LABELS AND MOUNTING															
[81]	FRONT PANEL USB - NESTED PCB															
[82]	BOM DEFINITIONS															
RULES: (APPLIED WHEN POSSIBLE)																
1. MSB TO LSB IS TOP TO BOTTOM																
2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT																
3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING																
4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS																
5. LANED SIGNALS ARE GROUPED ON SYMBOLS																
6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS																
7. SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES																
8. SUFFIX DP AND DN ARE USED FOR DIFFERENTIAL PAIRS																
9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE																
10.SUFFIX N FOR ACTIVE LOW OR N JUNCTION																
12.SUFFIX P FOR P JUNCTION																
13.SUFFIX EN FOR ENABLE																
14.'CLK' FOR CLOCKS, 'RST' FOR RESETS																
15.PWRGD FOR POWER GOOD																
16.REV AND FAB ARE SET USING CUSTOM VARIABLES																
TOOLS>OPTIONS>VARIABLES																
MICROSOFT PROJECT NAME PAGE CSA FAB VER																
CONFIDENTIAL Cactus 1/82 1/82 G-R 0.991																
8		7		6		5		4		3		2		1		

CACTUS

REV 0.991

FAB G RETAIL

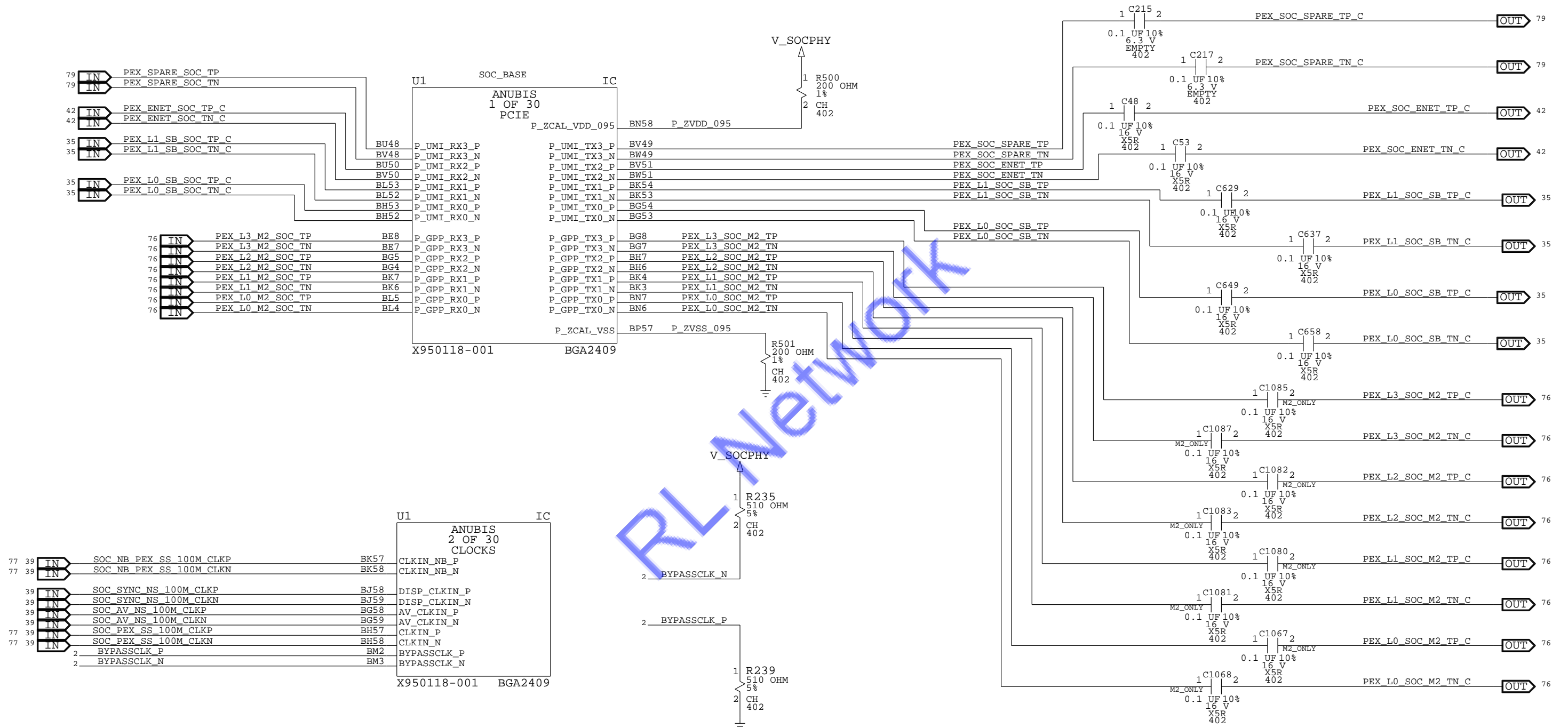
Thu Apr 20 16:18:47 2017

DRAWING

# SOC:PCIEX, CLOCKS

NOTES :

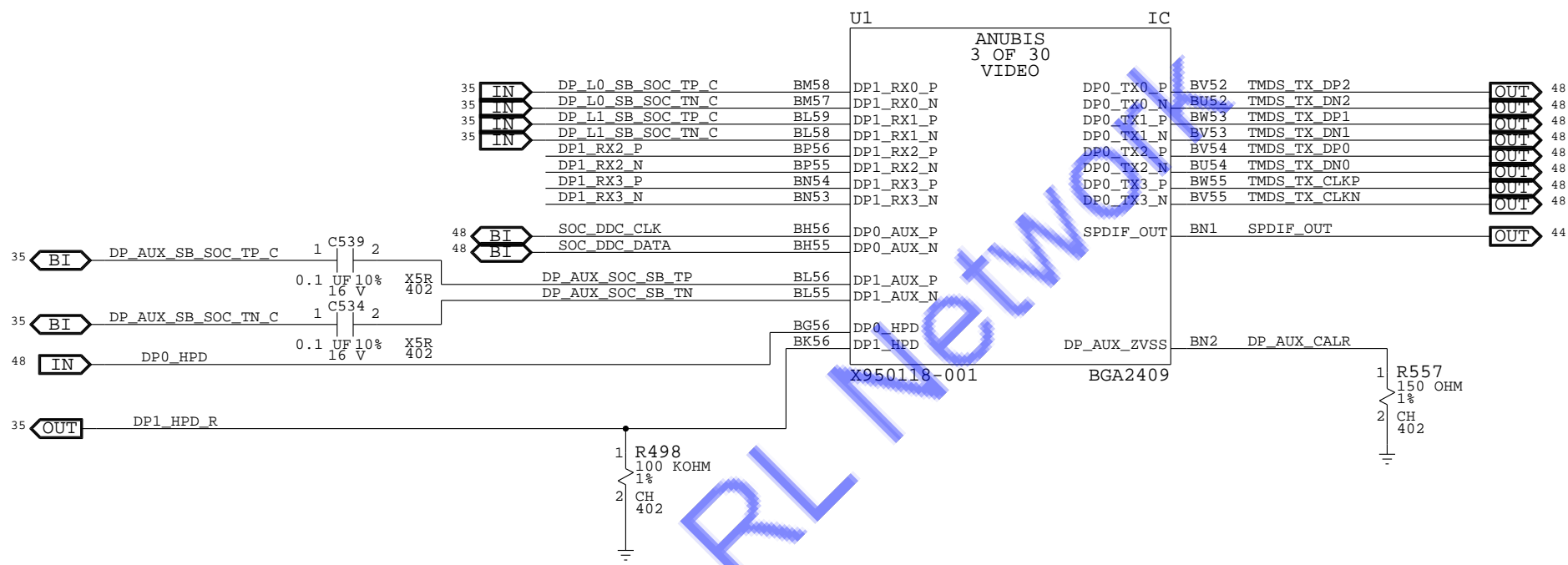
- 1.TO SUPPORT PCIE SPARE LANE INTERFACE (J28), POPULATE C215 AND C217
- 2.SEE PAGES 77 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X950118-001	IC	U1	PROCSS-CPU-GPU, SM, 1.0GHZ, BGA2049, ANUBIS1	SOC INCLUDE
X950118-001	EMPTY	U1	PROCSS-CPU-GPU, SM, 1.0GHZ, BGA2049, ANUBIS1	SOC EMPTY

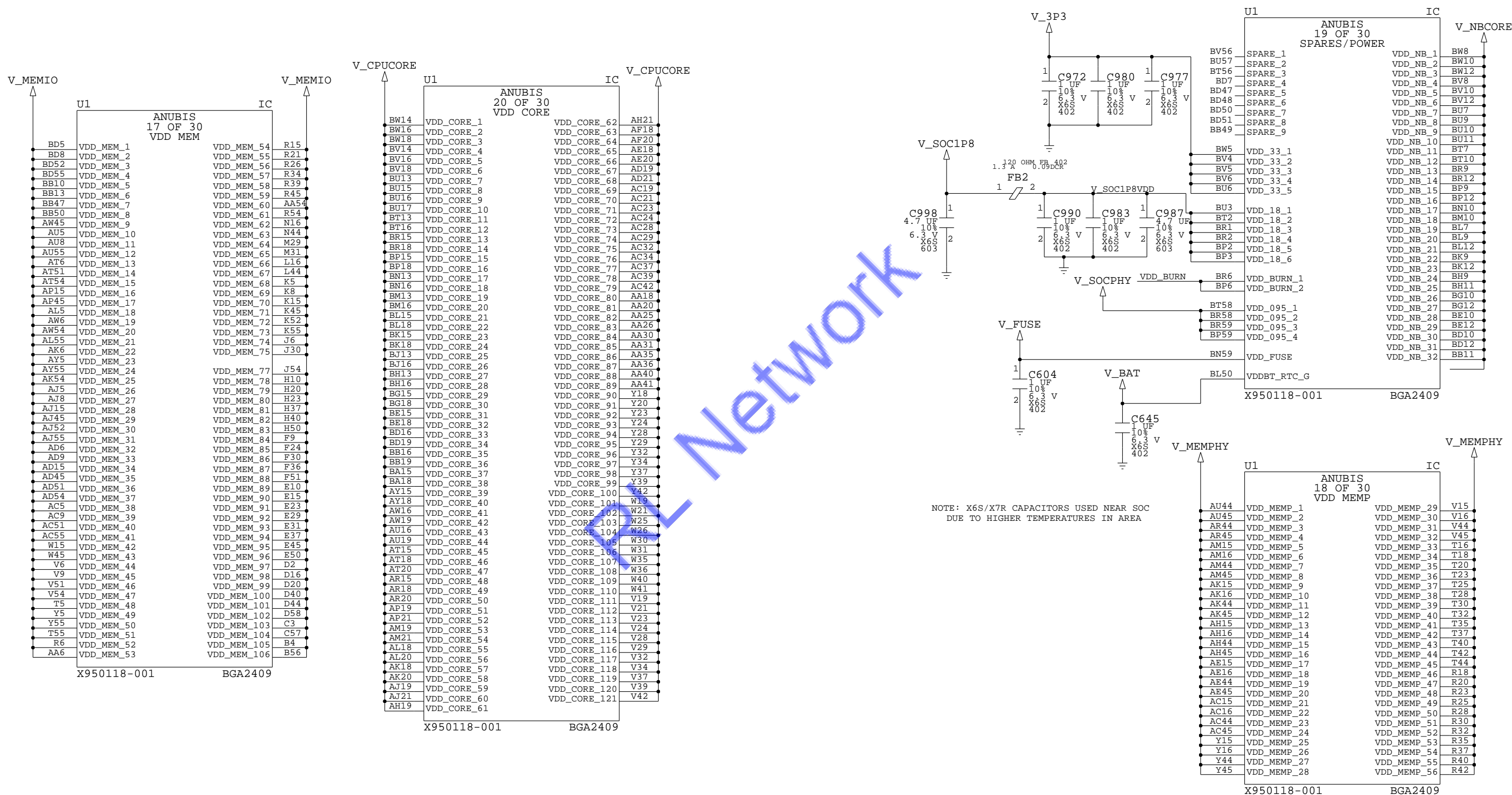
MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 2/82	CSA PAGE 2/82	FAB G-R	VER 0.991
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SOC: VIDEO



DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

SOC: POWER: MEMIO, MEMPHY, CPUCORE, NBCORE, MISC





SOC : POWER : GFXCORE

V\_GFXCORE

U1 ANUBIS 21 OF 30 VDD GFX IC

BW20 VDD\_GFX\_1 BT31  
BW22 VDD\_GFX\_2 BT34  
BW24 VDD\_GFX\_3 BT37  
BW26 VDD\_GFX\_4 BT40  
BW28 VDD\_GFX\_5 BT44  
BW30 VDD\_GFX\_6 BR21  
BW32 VDD\_GFX\_7 BR24  
BW34 VDD\_GFX\_8 BR27  
BW36 VDD\_GFX\_9 BR30  
BW38 VDD\_GFX\_10 BR33  
BW40 VDD\_GFX\_11 BR36  
BW42 VDD\_GFX\_12 BR39  
BW44 VDD\_GFX\_13 BR42  
BW45 VDD\_GFX\_14 BR45  
BV20 VDD\_GFX\_15 BP21  
BV22 VDD\_GFX\_16 BP24  
BV24 VDD\_GFX\_17 BP27  
BV26 VDD\_GFX\_18 BP30  
BV28 VDD\_GFX\_19 BP33  
BV30 VDD\_GFX\_20 BP36  
BV32 VDD\_GFX\_21 BP39  
BV34 VDD\_GFX\_22 BP42  
BV36 VDD\_GFX\_23 BP45  
BV38 VDD\_GFX\_24 BN20  
BV40 VDD\_GFX\_25 BN23  
BV42 VDD\_GFX\_26 BN26  
BV44 VDD\_GFX\_27 BN29  
BV45 VDD\_GFX\_28 BN31  
BU19 VDD\_GFX\_29 BN34  
BU20 VDD\_GFX\_30 BN37  
BU22 VDD\_GFX\_31 BN40  
BU23 VDD\_GFX\_32 BN44  
BU25 VDD\_GFX\_33 BM20  
BU26 VDD\_GFX\_34 BM23  
BU28 VDD\_GFX\_35 BM26  
BU29 VDD\_GFX\_36 BM29  
BU31 VDD\_GFX\_37 BM31  
BU32 VDD\_GFX\_38 BM34  
BU34 VDD\_GFX\_39 BM37  
BU35 VDD\_GFX\_40 BM40  
BU37 VDD\_GFX\_41 BM44  
BU38 VDD\_GFX\_42 BL21  
BU40 VDD\_GFX\_43 BL24  
BU41 VDD\_GFX\_44 BL27  
BU43 VDD\_GFX\_45 BL30  
BU44 VDD\_GFX\_46 BL33  
BT20 VDD\_GFX\_47 BL36  
BT23 VDD\_GFX\_48 BL39  
BT26 VDD\_GFX\_49 BL42  
BT29 VDD\_GFX\_50 BL45

V\_GFXCORE

X950118-001 BGA2409

V\_GFXCORE

U1 ANUBIS 22 OF 30 VDD GFX IC

BK21 VDD\_GFX\_101 BD29  
BK24 VDD\_GFX\_102 BD31  
BK27 VDD\_GFX\_103 BD34  
BK30 VDD\_GFX\_104 BD36  
BK33 VDD\_GFX\_105 BD39  
BK36 VDD\_GFX\_106 BD41  
BK39 VDD\_GFX\_107 BD44  
BK42 VDD\_GFX\_108 BB21  
BK45 VDD\_GFX\_109 BB24  
BJ20 VDD\_GFX\_110 BB26  
BJ23 VDD\_GFX\_111 BB29  
BJ26 VDD\_GFX\_112 BB31  
BJ29 VDD\_GFX\_113 BB34  
BJ31 VDD\_GFX\_114 BB36  
BJ34 VDD\_GFX\_115 BB39  
BJ37 VDD\_GFX\_116 BB41  
BJ40 VDD\_GFX\_117 BB44  
BJ44 VDD\_GFX\_118 BA20  
BH20 VDD\_GFX\_119 BA23  
BH23 VDD\_GFX\_120 BA25  
BH26 VDD\_GFX\_121 BA28  
BH29 VDD\_GFX\_122 BA30  
BH31 VDD\_GFX\_123 BA32  
BH34 VDD\_GFX\_124 BA35  
BH37 VDD\_GFX\_125 BA37  
BH40 VDD\_GFX\_126 BA40  
BH44 VDD\_GFX\_127 BA42  
BG21 VDD\_GFX\_128 BA45  
BG24 VDD\_GFX\_129 AY20  
BG27 VDD\_GFX\_130 AY23  
BG30 VDD\_GFX\_131 AY25  
BG33 VDD\_GFX\_132 AY28  
BG36 VDD\_GFX\_133 AY30  
BG39 VDD\_GFX\_134 AY32  
BG42 VDD\_GFX\_135 AY35  
BG45 VDD\_GFX\_136 AY37  
BE20 VDD\_GFX\_137 AY40  
BE23 VDD\_GFX\_138 AY42  
BE25 VDD\_GFX\_139 AY45  
BE28 VDD\_GFX\_140 AW21  
BE30 VDD\_GFX\_141 AW24  
BE32 VDD\_GFX\_142 AW26  
BE35 VDD\_GFX\_143 AW29  
BE37 VDD\_GFX\_144 AW31  
BE40 VDD\_GFX\_145 AW34  
BE42 VDD\_GFX\_146 AW36  
BE45 VDD\_GFX\_147 AW39  
BD21 VDD\_GFX\_148 AW41  
BD24 VDD\_GFX\_149 AU21  
BD26 VDD\_GFX\_150 AU24

V\_GFXCORE

X950118-001 BGA2409

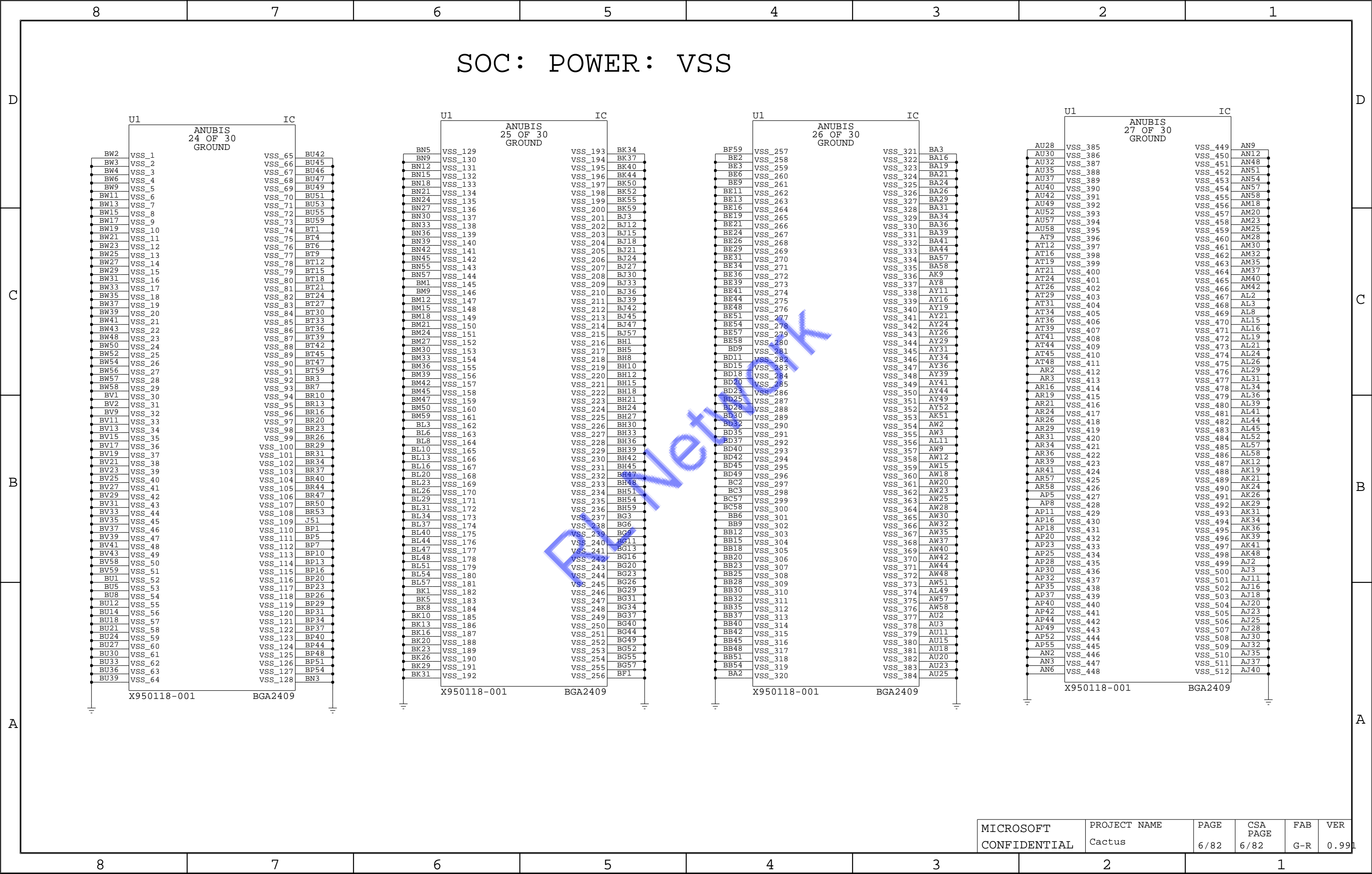
V\_GFXCORE

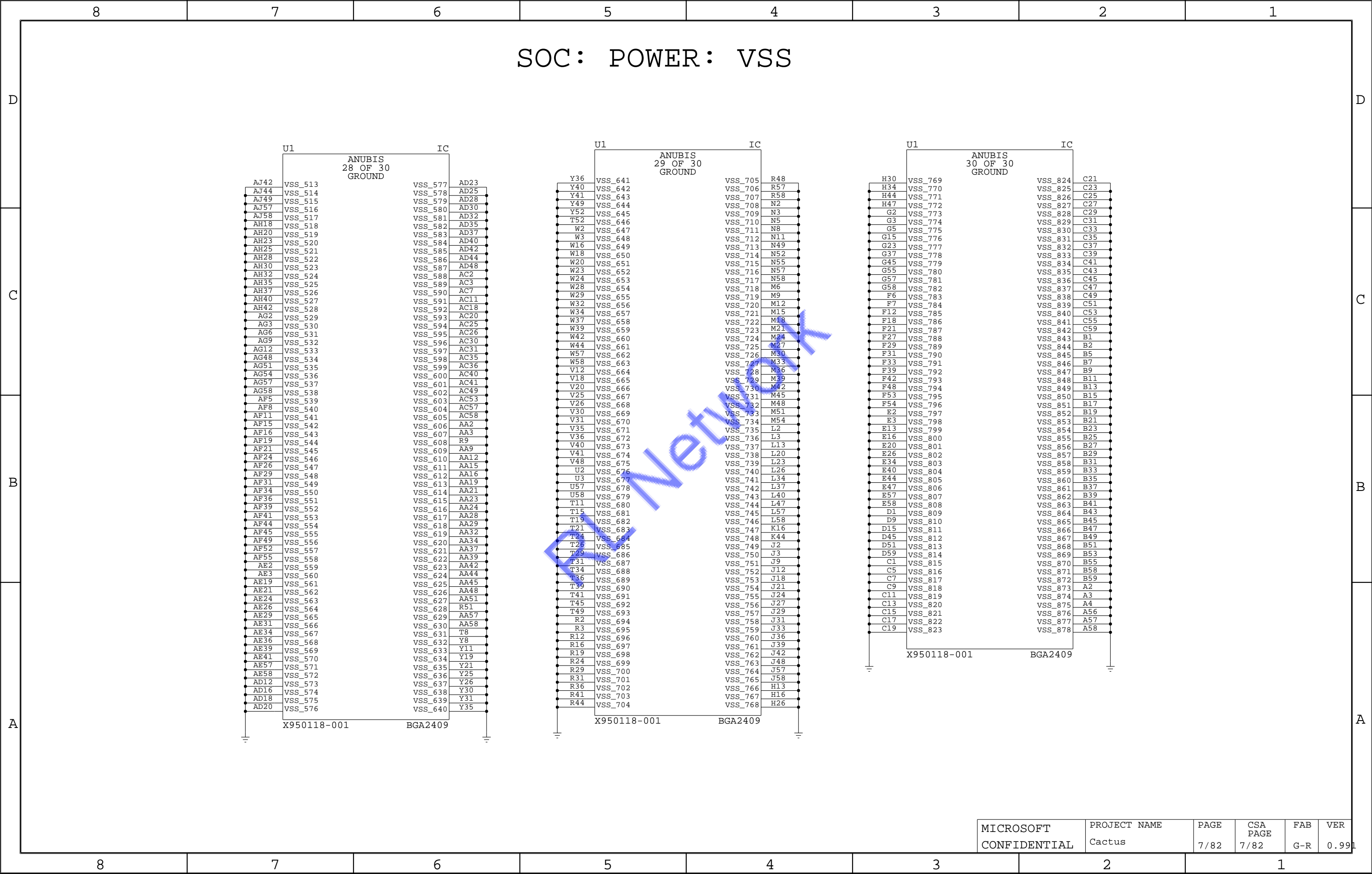
U1 ANUBIS 23 OF 30 VDD GFX IC

AU26 VDD\_GFX\_201 AK23  
AU29 VDD\_GFX\_202 AK25  
AU31 VDD\_GFX\_203 AK28  
AU34 VDD\_GFX\_204 AK30  
AU36 VDD\_GFX\_205 AK32  
AU39 VDD\_GFX\_206 AK35  
AU41 VDD\_GFX\_207 AK37  
AT23 VDD\_GFX\_208 AK40  
AT25 VDD\_GFX\_209 AK42  
AT28 VDD\_GFX\_210 AJ24  
AT30 VDD\_GFX\_211 AJ26  
AT32 VDD\_GFX\_212 AJ29  
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AT40 VDD\_GFX\_215 AJ36  
AT42 VDD\_GFX\_216 AJ39  
AR23 VDD\_GFX\_217 AH24  
AR25 VDD\_GFX\_218 AH26  
AR28 VDD\_GFX\_219 AH29  
AR30 VDD\_GFX\_220 AH31  
AR32 VDD\_GFX\_221 AH34  
AR35 VDD\_GFX\_222 AH36  
AR37 VDD\_GFX\_223 AH39  
AR40 VDD\_GFX\_224 AH41  
AR42 VDD\_GFX\_225 AF23  
AP24 VDD\_GFX\_226 AF25  
AP26 VDD\_GFX\_227 AF28  
AP29 VDD\_GFX\_228 AF30  
AP31 VDD\_GFX\_229 AF32  
AP34 VDD\_GFX\_230 AF35  
AP36 VDD\_GFX\_231 AF37  
AP39 VDD\_GFX\_232 AF40  
AP41 VDD\_GFX\_233 AF42  
AM24 VDD\_GFX\_234 AE23  
AM26 VDD\_GFX\_235 AE25  
AM29 VDD\_GFX\_236 AE28  
AM31 VDD\_GFX\_237 AE30  
AM34 VDD\_GFX\_238 AE32  
AM36 VDD\_GFX\_239 AE35  
AM39 VDD\_GFX\_240 AE37  
AM41 VDD\_GFX\_241 AE40  
AL23 VDD\_GFX\_242 AE42  
AL25 VDD\_GFX\_243 AD24  
AL28 VDD\_GFX\_244 AD26  
AL30 VDD\_GFX\_245 AD29  
AL32 VDD\_GFX\_246 AD31  
AL35 VDD\_GFX\_247 AD34  
AL37 VDD\_GFX\_248 AD36  
AL40 VDD\_GFX\_249 AD39  
AL42 VDD\_GFX\_250 AD41

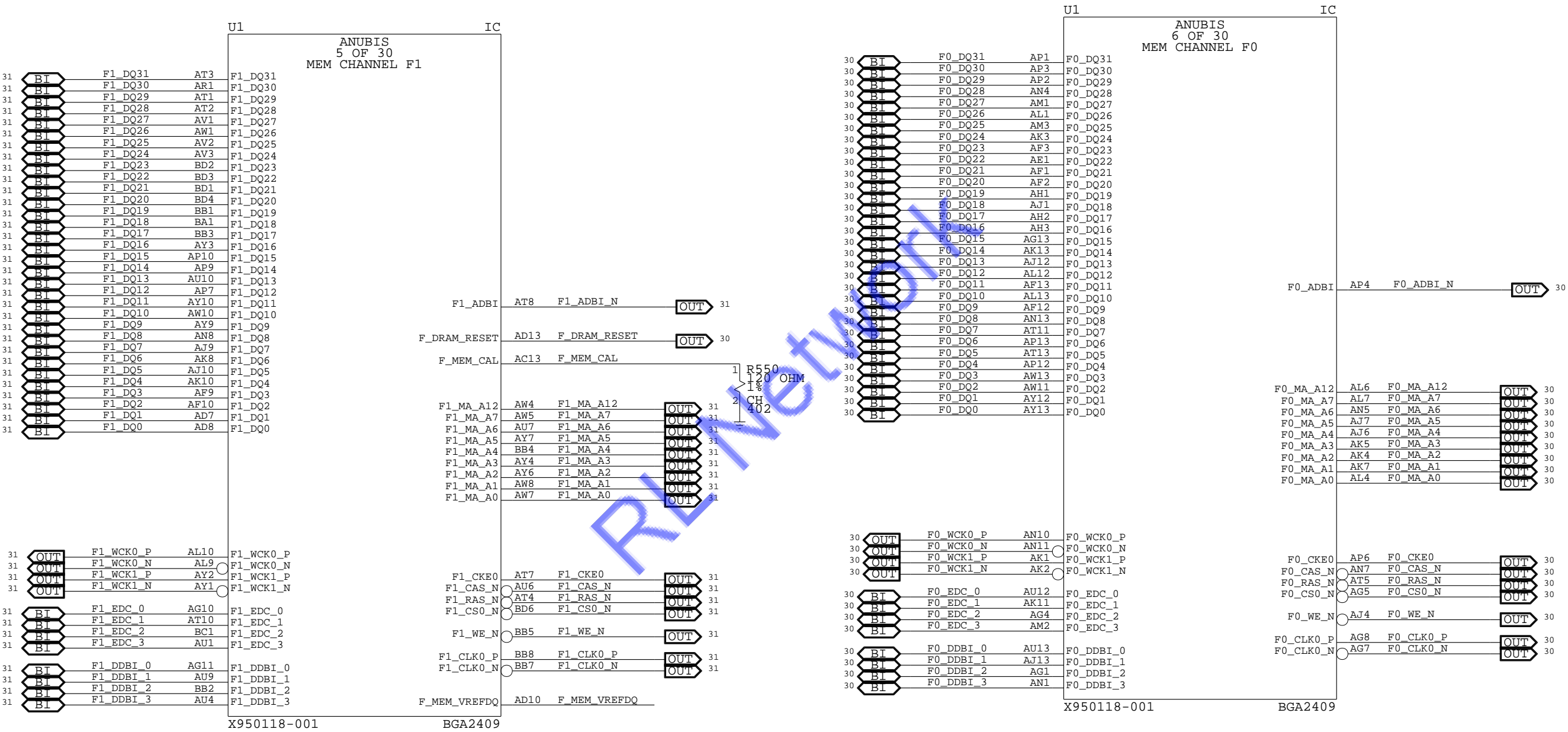
V\_GFXCORE

X950118-001 BGA2409



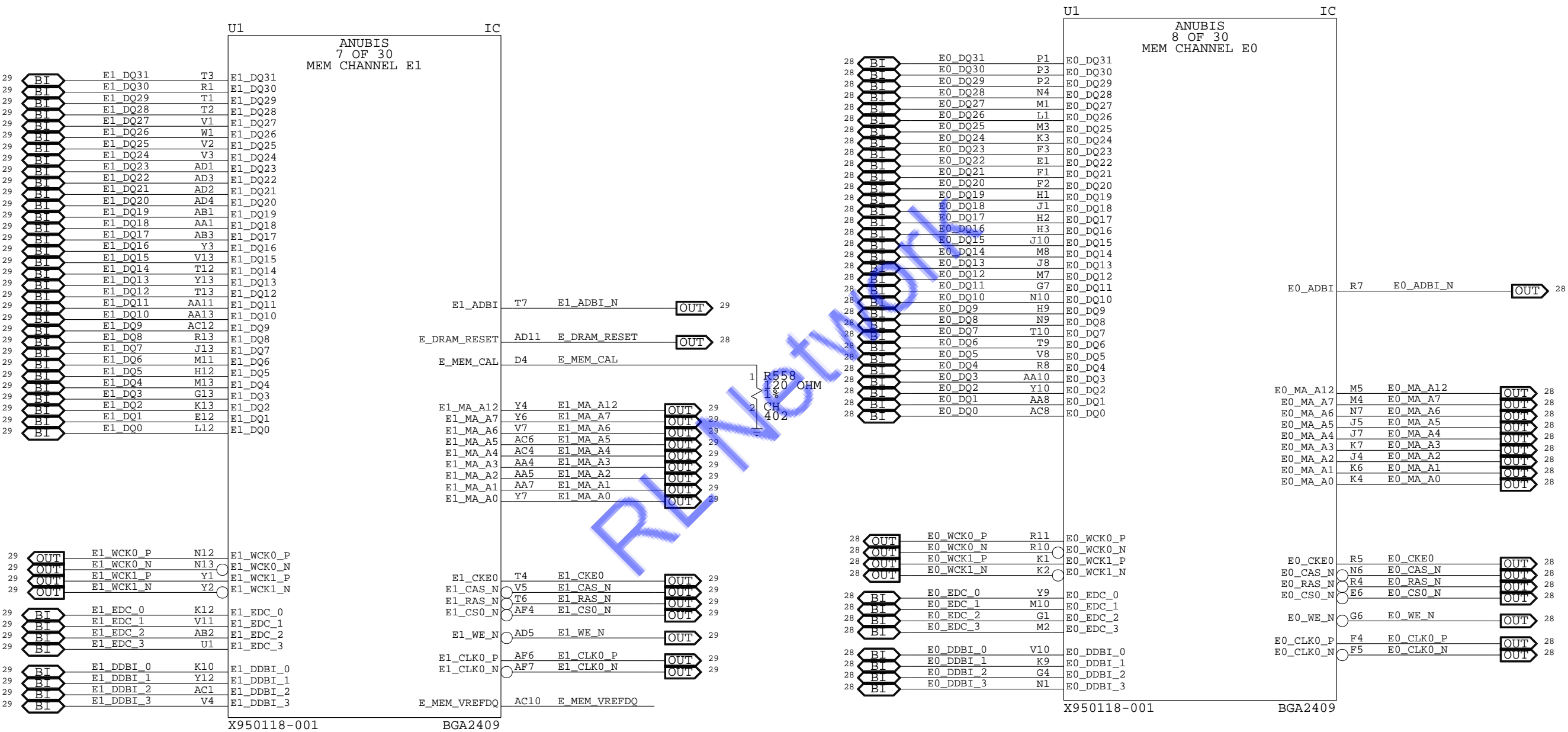


MEMORY: PARTITION F1/F0

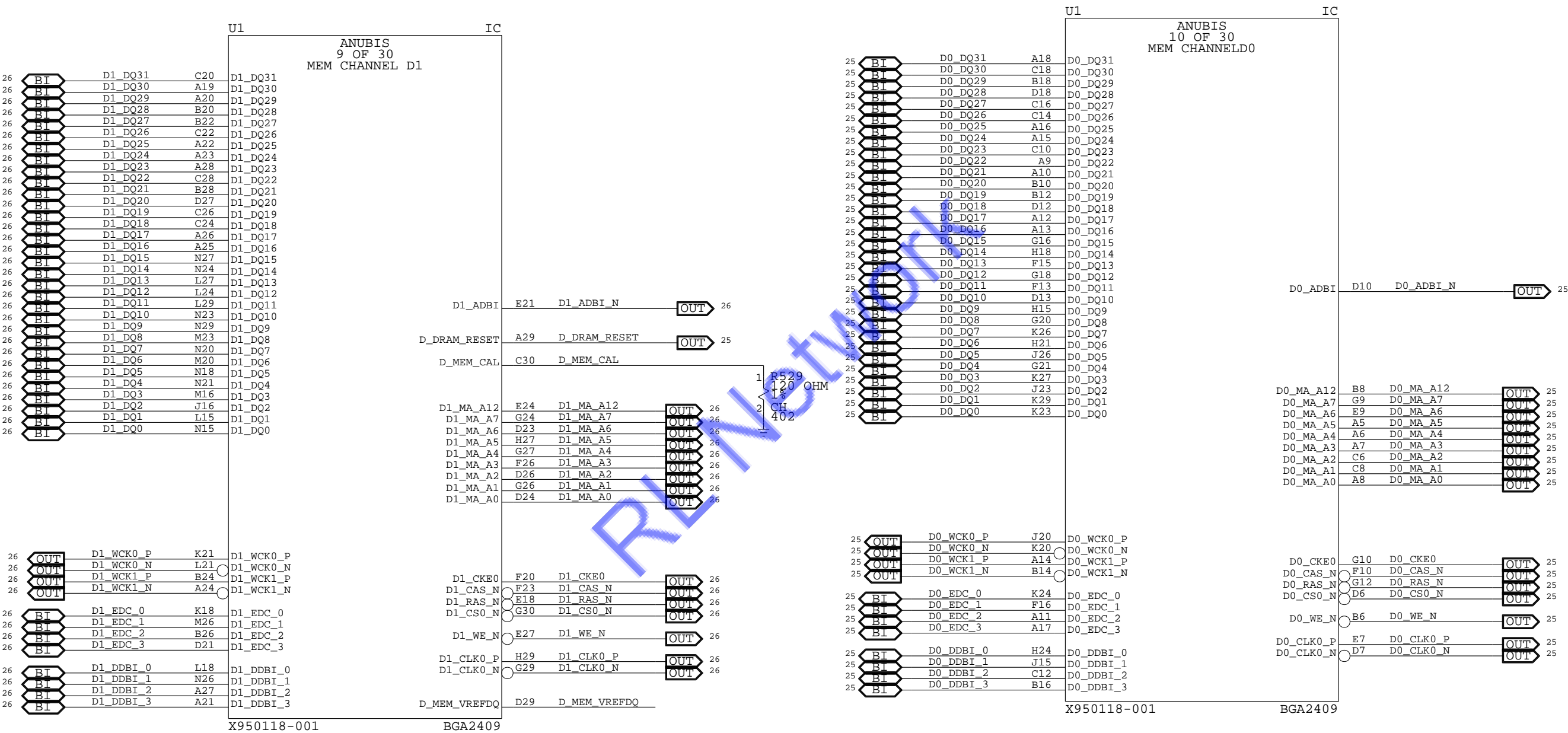




MEMORY: PARTITION E1/E0



MEMORY: PARTITION D1/D0



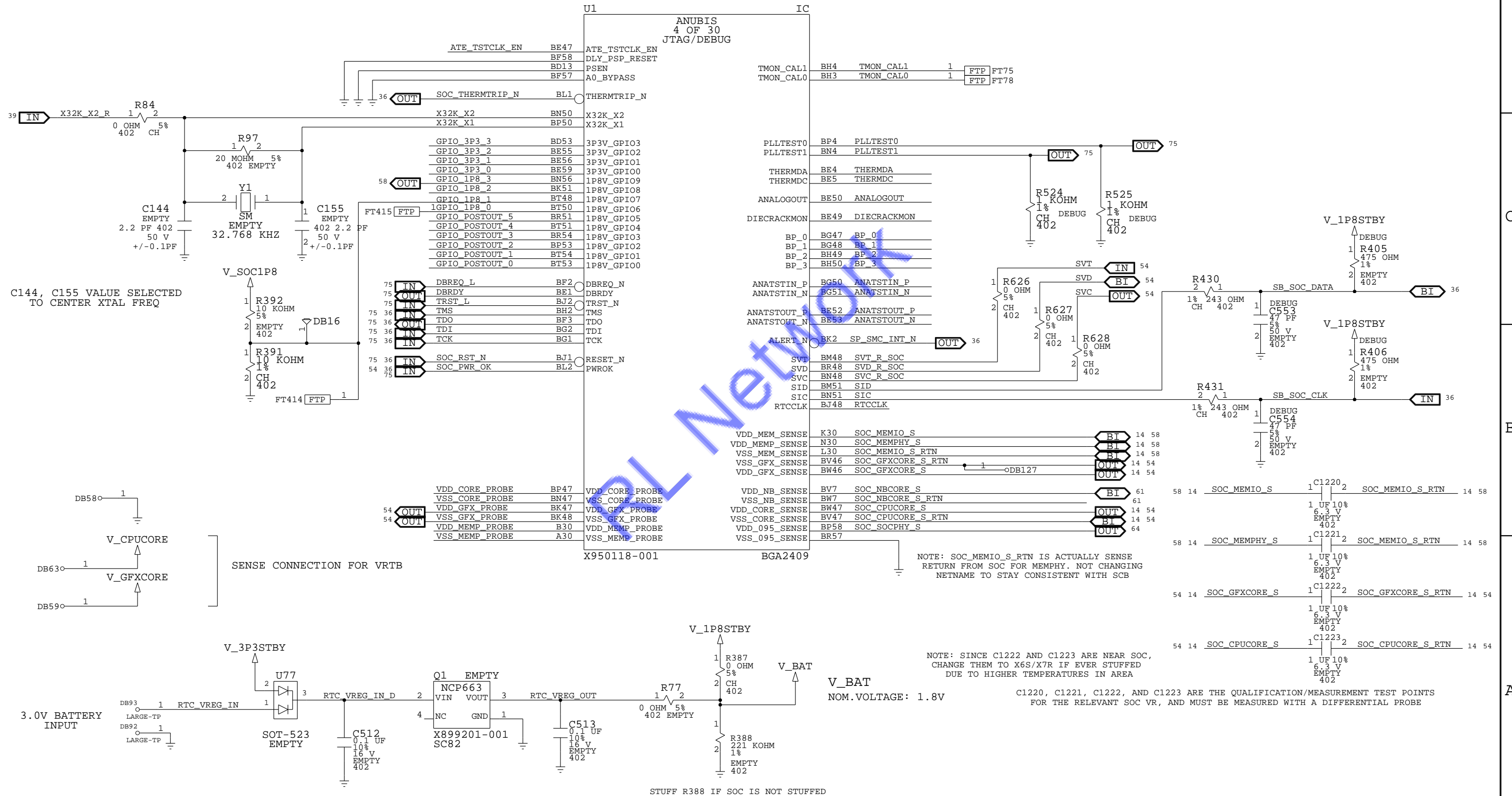
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[illegible]



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## SOC:DEBUG,SB SIGNALS,V\_BAT



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SOC: DECOUPLING

D

C

B

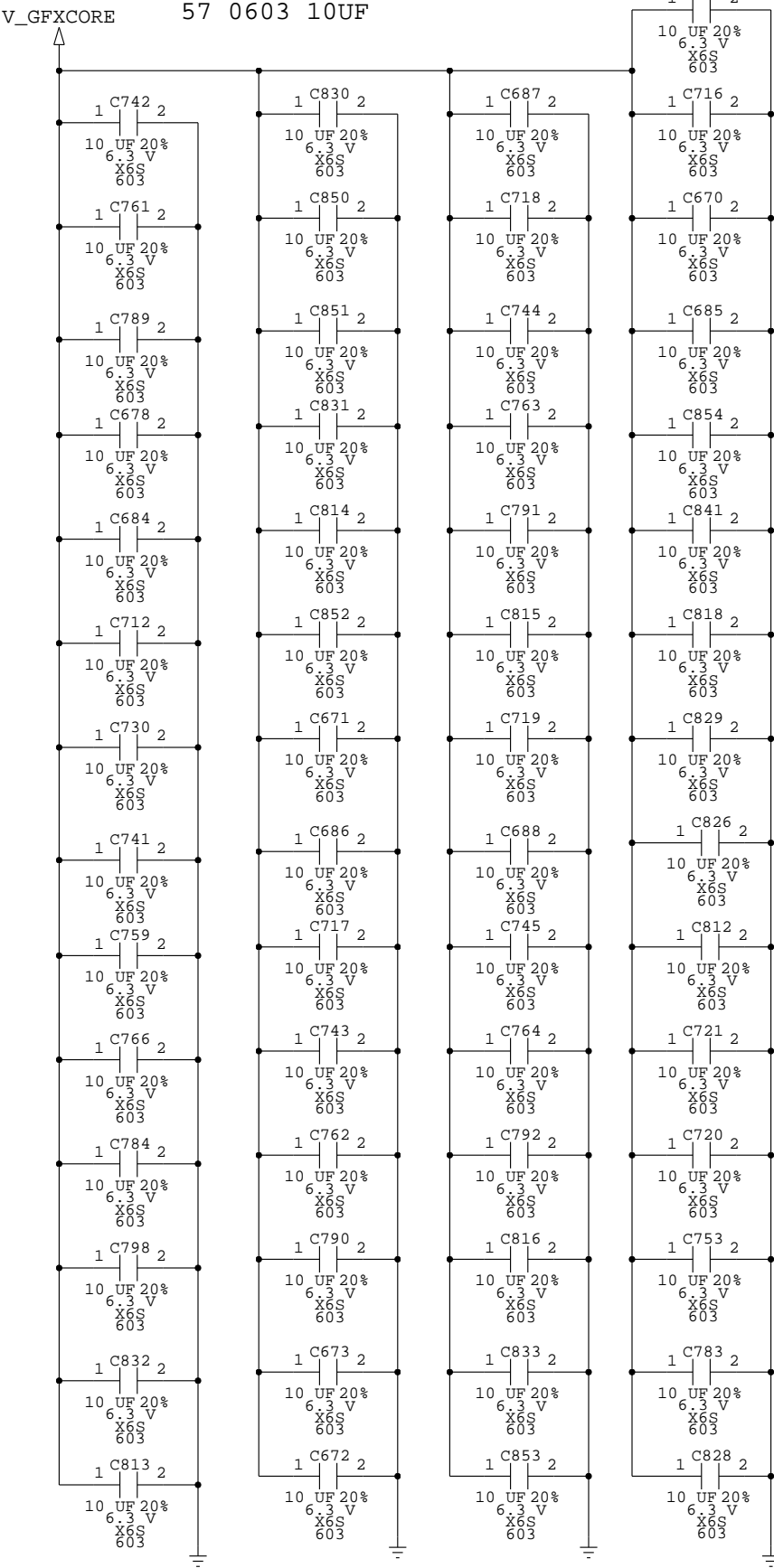
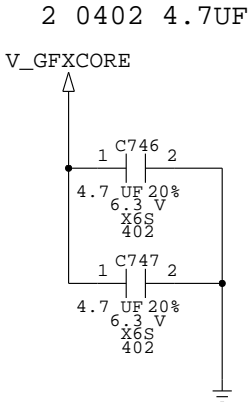
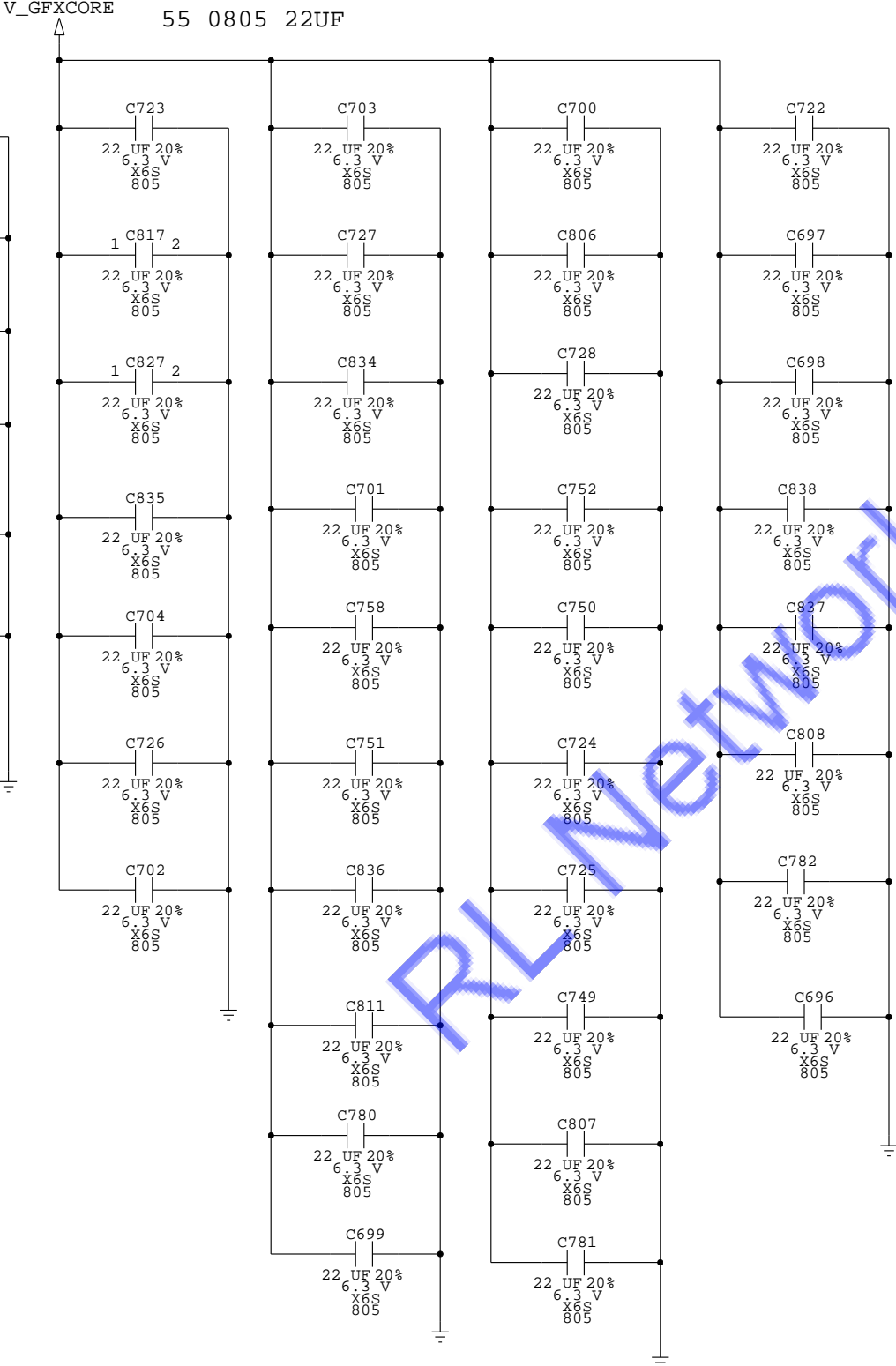
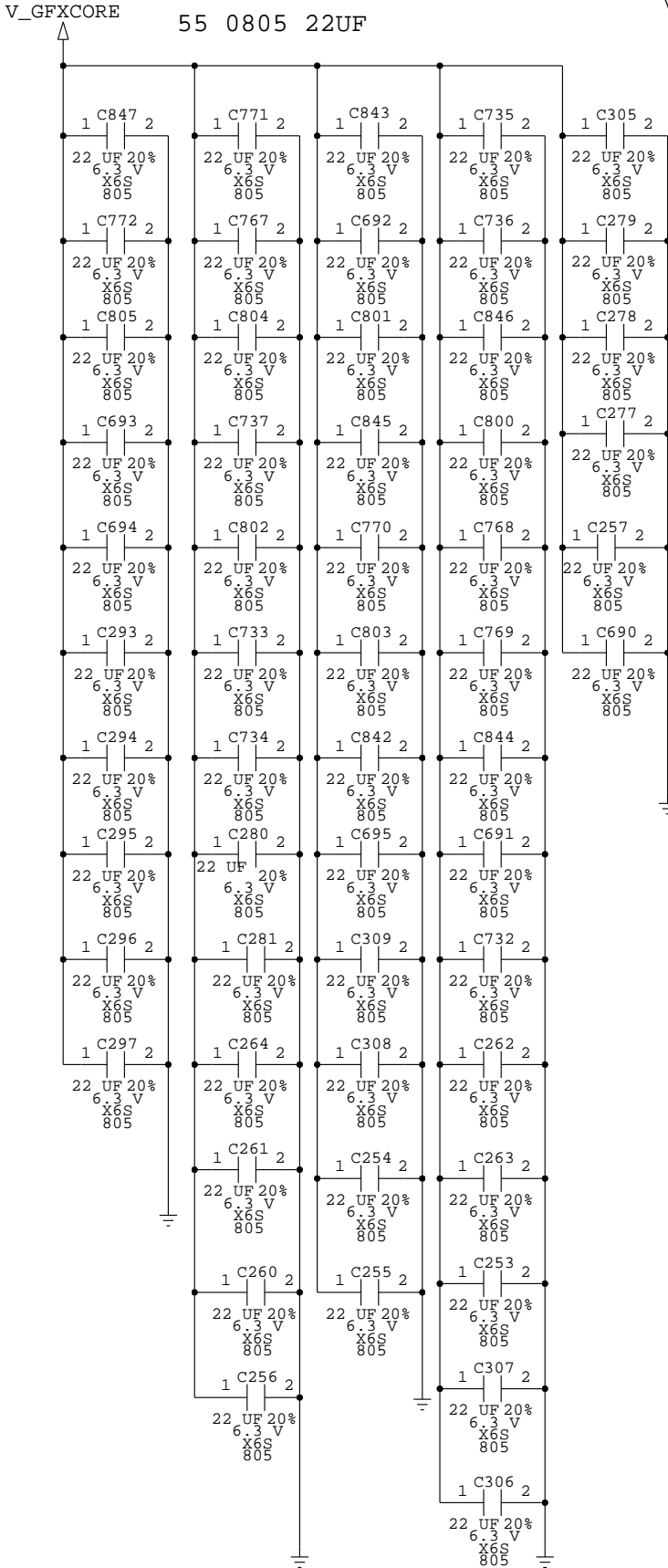
A

D

C

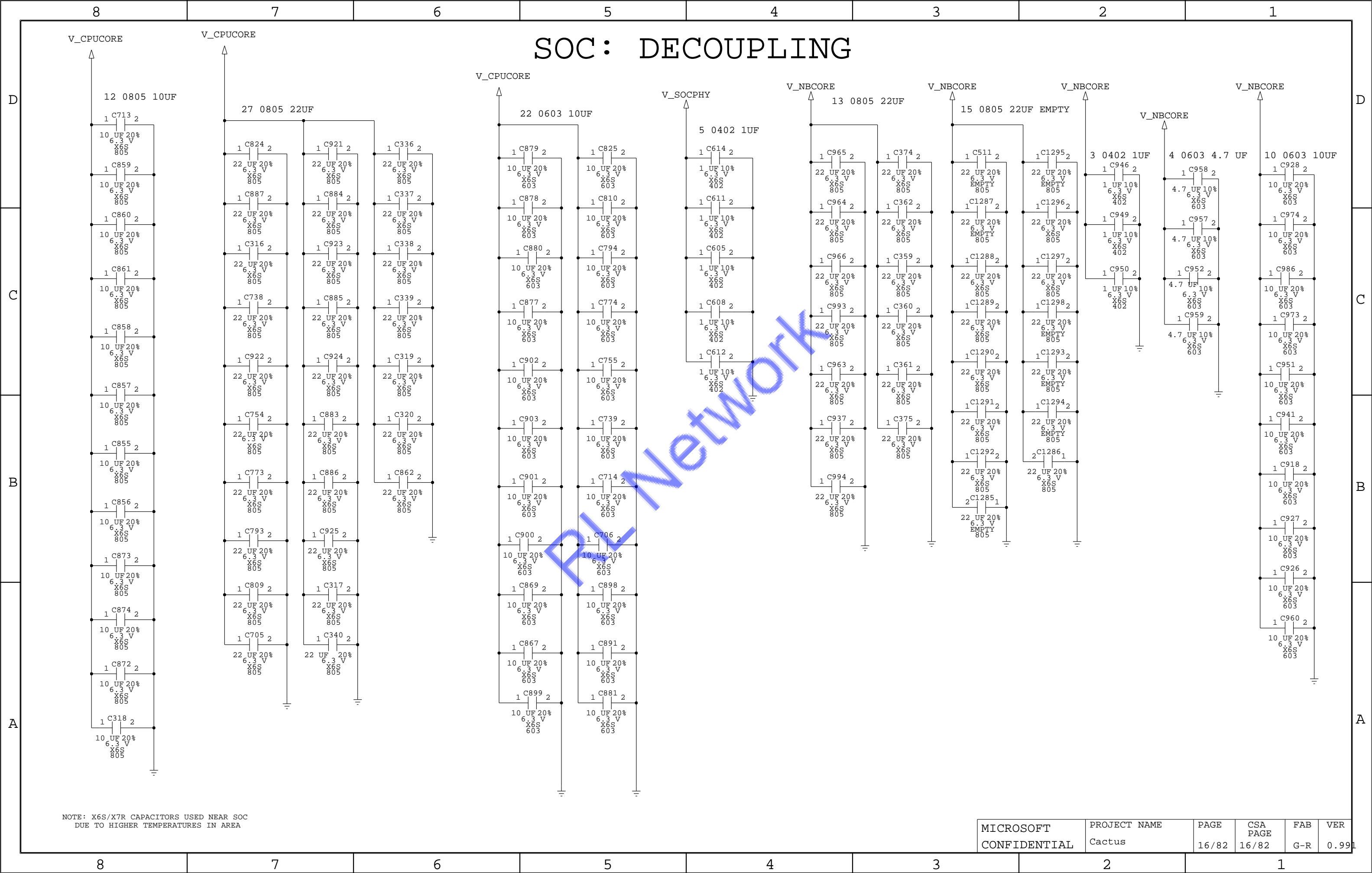
B

A



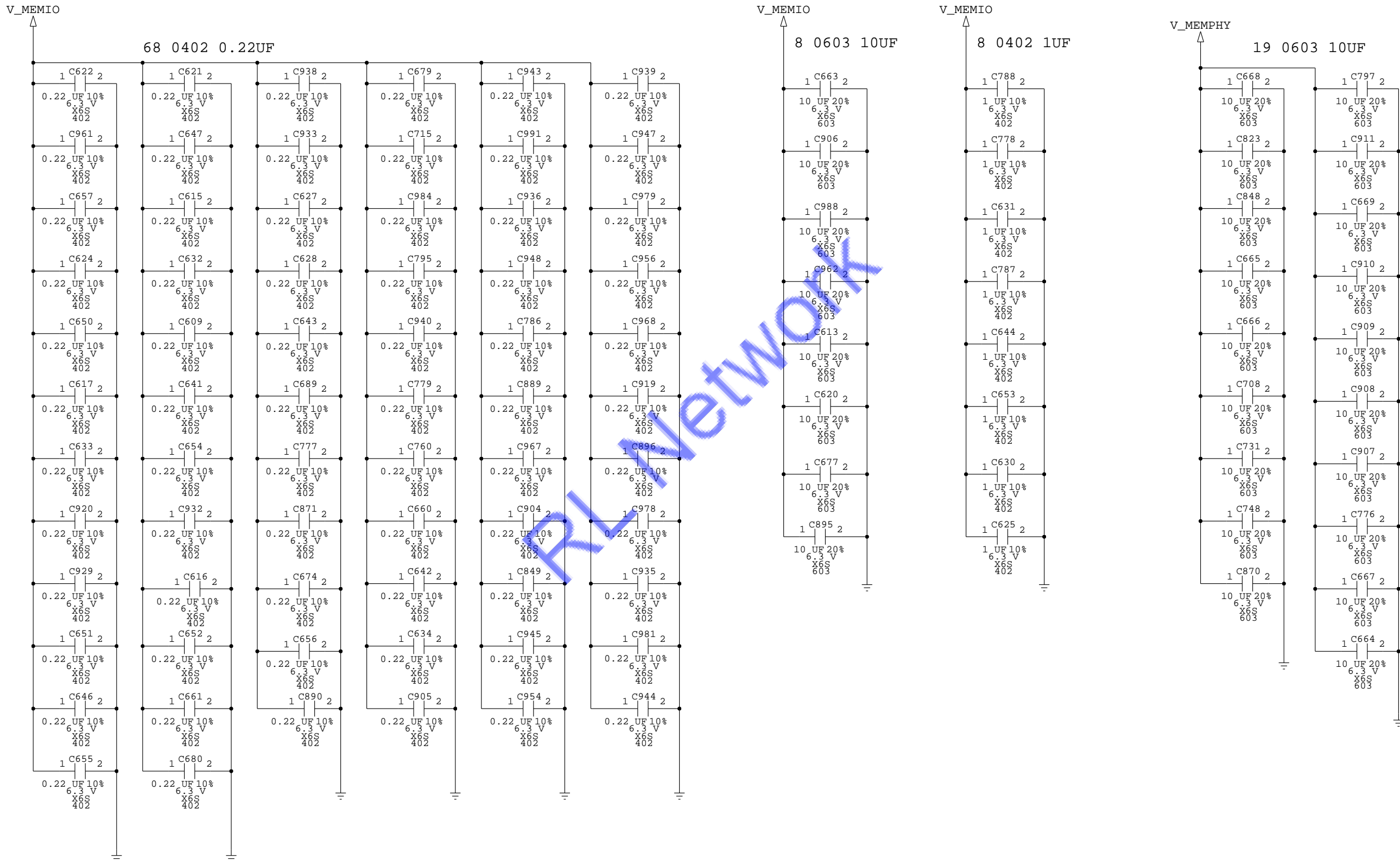
NOTE: X6S/X7R CAPACITORS USED NEAR SOC  
DUE TO HIGHER TEMPERATURES IN AREA

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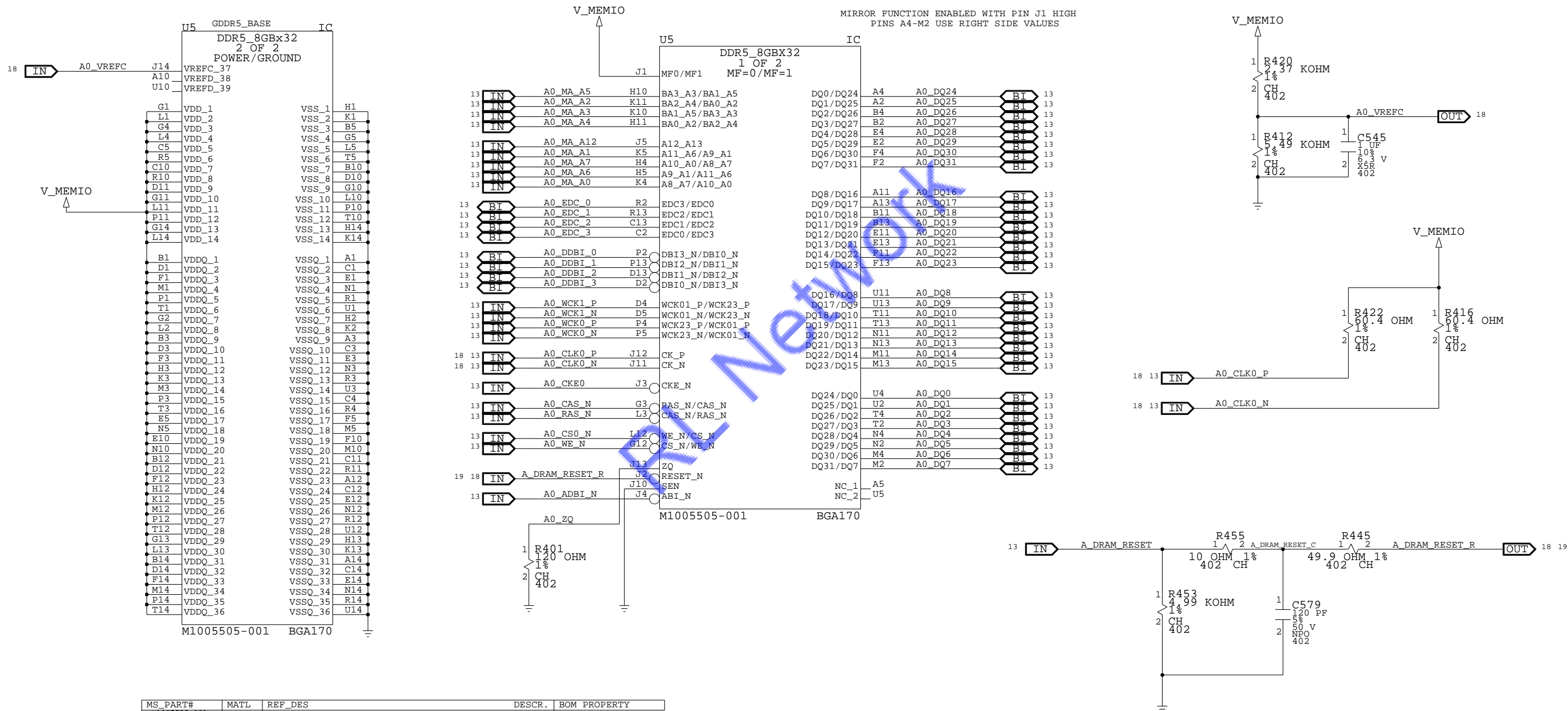
## SOC: DECOUPLING



NOTE: X6S/X7R CAPACITORS USED NEAR SOC  
DUE TO HIGHER TEMPERATURES IN AREA

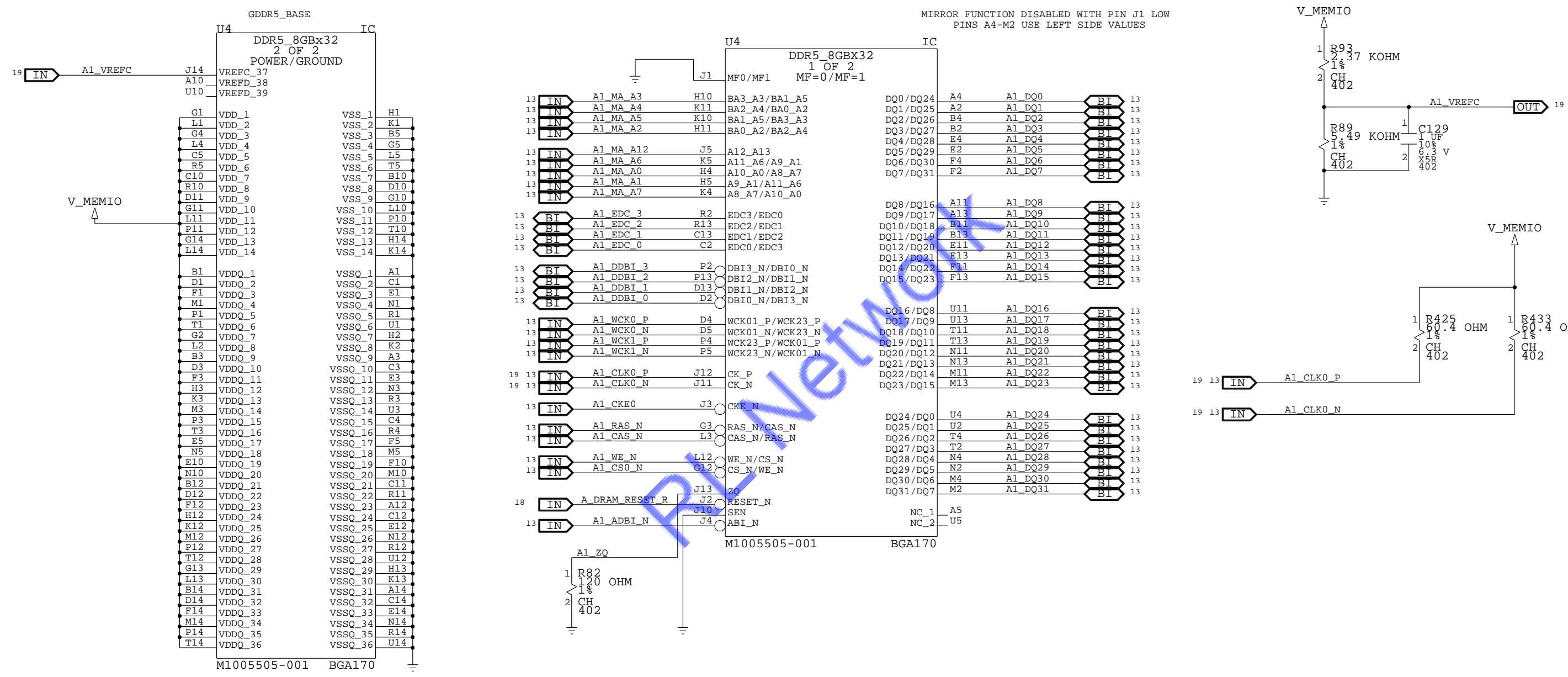
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
CONFIDENTIAL	Cactus	17/82	17/82	G-R	0.991

MEMORY: CHANNEL A0

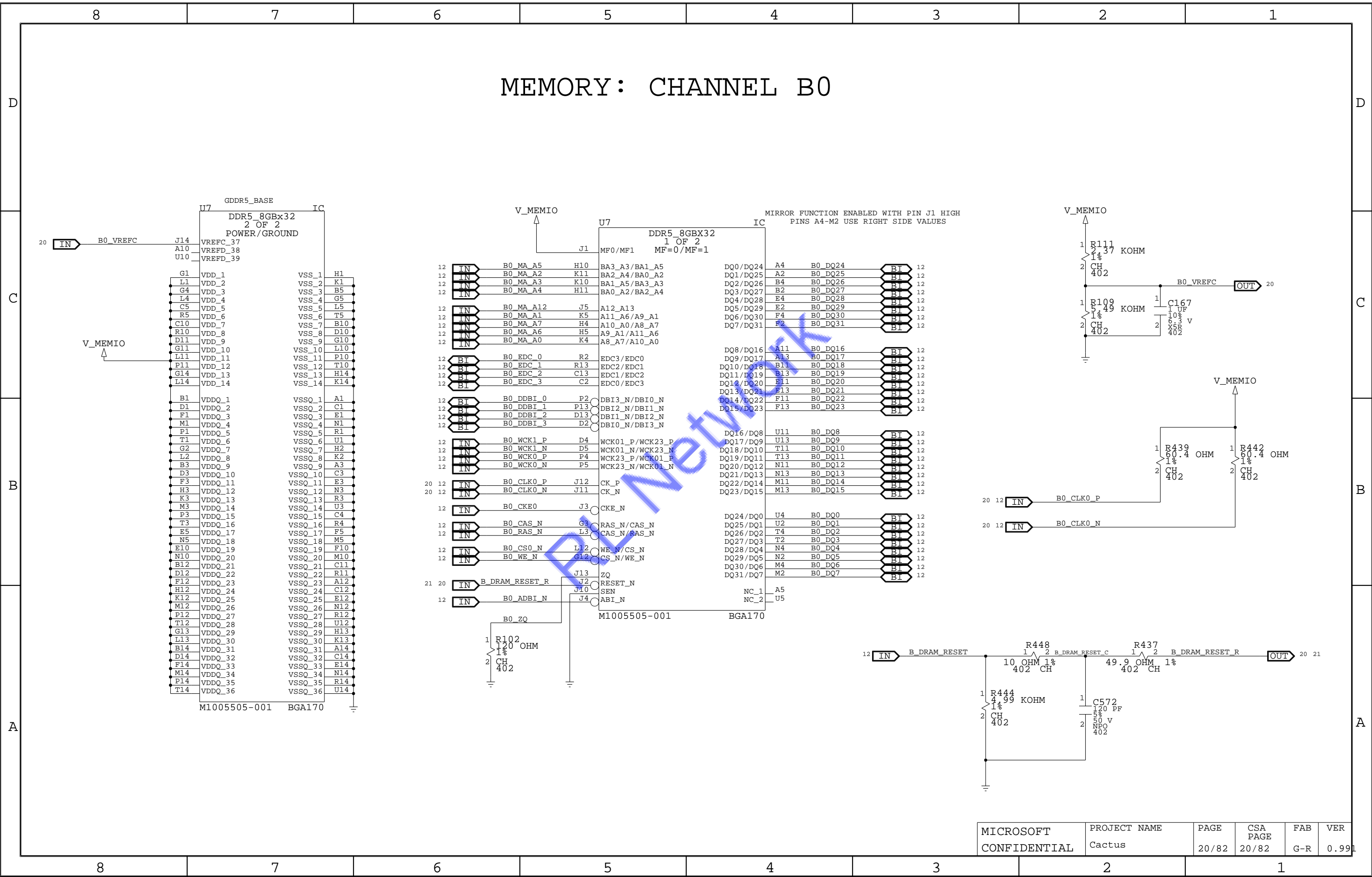


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M1005505-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FPBGA	GDDR5_SAMSUNG
M1005717-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FPBGA	GDDR5_HYNIX

MEMORY: CHANNEL A1



MEMORY: CHANNEL B0





8 7 6 5 4 3 2 1

D

C

B

A

8 7 6 5 4 3 2 1

D

C

B

A

MEMORY: CHANNEL B1

U6 GDDR5\_BASE IC

DDR5\_8GBx32 2 OF 2 POWER/GROUND

VREFC\_37 VREFD\_38 VREFD\_39

B1\_VREFC J14

V\_MEMIO

U6 IC

DDR5\_8GBX32 1 OF 2 MF0/MF1 MF=0/MF=1

J1

B1\_MA A3 H10 BA3\_A3/BA1\_A5 DQ0/DQ24 A4 B1 DQ0 BT 12

B1\_MA A4 K11 BA2\_A4/BA0\_A2 DQ1/DQ25 A2 B1 DQ1 BT 12

B1\_MA A5 K10 BA1\_A5/BA3\_A3 DQ2/DQ26 B4 B1 DQ2 BT 12

B1\_MA A2 H11 BA0\_A2/BA2\_A4 DQ3/DQ27 B2 B1 DQ3 BT 12

B1\_MA A12 J5 A12\_A13 DQ4/DQ28 E4 B1 DQ4 BT 12

B1\_MA A6 K5 A11\_A6/A9\_A1 DQ5/DQ29 E2 B1 DQ5 BT 12

B1\_MA A0 H4 A10\_A0/A8\_A7 DQ6/DQ30 F4 B1 DQ6 BT 12

B1\_MA A1 H5 A9\_A1/A11\_A6 DQ7/DQ31 F2 B1 DQ7 BT 12

B1\_MA A7 K4 A8\_A7/A10\_A0

B1\_EDC 3 R2 EDC3/EDC0 DQ8/DQ16 A11 B1 DQ8 BT 12

B1\_EDC 2 R13 EDC2/EDC1 DQ9/DQ17 A13 B1 DQ9 BT 12

B1\_EDC 1 C13 EDC1/EDC2 DQ10/DQ18 B11 B1 DQ10 BT 12

B1\_EDC 0 C2 EDC0/EDC3 DQ11/DQ19 B13 B1 DQ11 BT 12

B1\_DDBI 3 P2 DBI3\_N/DBI0\_N DQ12/DQ20 E11 B1 DQ12 BT 12

B1\_DDBI 2 P13 DBI2\_N/DBI1\_N DQ13/DQ21 E13 B1 DQ13 BT 12

B1\_DDBI 1 D13 DBI1\_N/DBI2\_N DQ14/DQ22 F11 B1 DQ14 BT 12

B1\_DDBI 0 D2 DBI0\_N/DBI3\_N DQ15/DQ23 F13 B1 DQ15 BT 12

B1\_WCK0\_P D4 WCK01\_P/WCK23\_P DQ16/DQ8 U11 B1 DQ16 BT 12

B1\_WCK0\_N D5 WCK01\_N/WCK23\_N DQ17/DQ9 U13 B1 DQ17 BT 12

B1\_WCK1\_P P4 WCK23\_P/WCK01\_P DQ18/DQ10 T11 B1 DQ18 BT 12

B1\_WCK1\_N P5 WCK23\_N/WCK01\_N DQ19/DQ11 T13 B1 DQ19 BT 12

B1\_CLK0\_P J12 CK\_P DQ20/DQ12 N11 B1 DQ20 BT 12

B1\_CLK0\_N J11 CK\_N DQ21/DQ13 N13 B1 DQ21 BT 12

B1\_CKE0 J3 CKE\_N DQ22/DQ14 M11 B1 DQ22 BT 12

B1\_RAS\_N G3 RAS\_N/CAS\_N DQ23/DQ15 M13 B1 DQ23 BT 12

B1\_CAS\_N L3 CAS\_N/RAS\_N

B1\_WE\_N L12 WE\_N/CS\_N DQ24/DQ0 U4 B1 DQ24 BT 12

B1\_CS0\_N G12 CS\_N/WE\_N DQ25/DQ1 U2 B1 DQ25 BT 12

B\_DRAM\_RESET\_R J13 ZQ DQ26/DQ2 T4 B1 DQ26 BT 12

B1\_ADBI\_N J10 SEN DQ27/DQ3 T2 B1 DQ27 BT 12

B1\_ZQ R399 120 OHM DQ28/DQ4 N4 B1 DQ28 BT 12

J4 ABI\_N DQ29/DQ5 N2 B1 DQ29 BT 12

M1005505-001 BGA170 DQ30/DQ6 M4 B1 DQ30 BT 12

NC\_1 A5 DQ31/DQ7 M2 B1 DQ31 BT 12

NC\_2 U5

V\_MEMIO

B1\_VREFC

B1\_VREFC

B1\_CLK0\_P

B1\_CLK0\_N

R409 1.37 KOHM

CH 402

R402 5.49 KOHM

CH 402

C537 10UF

6.3V

R414 60.4 OHM

CH 402

R415 60.4 OHM

CH 402

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PROJECT NAME Cactus

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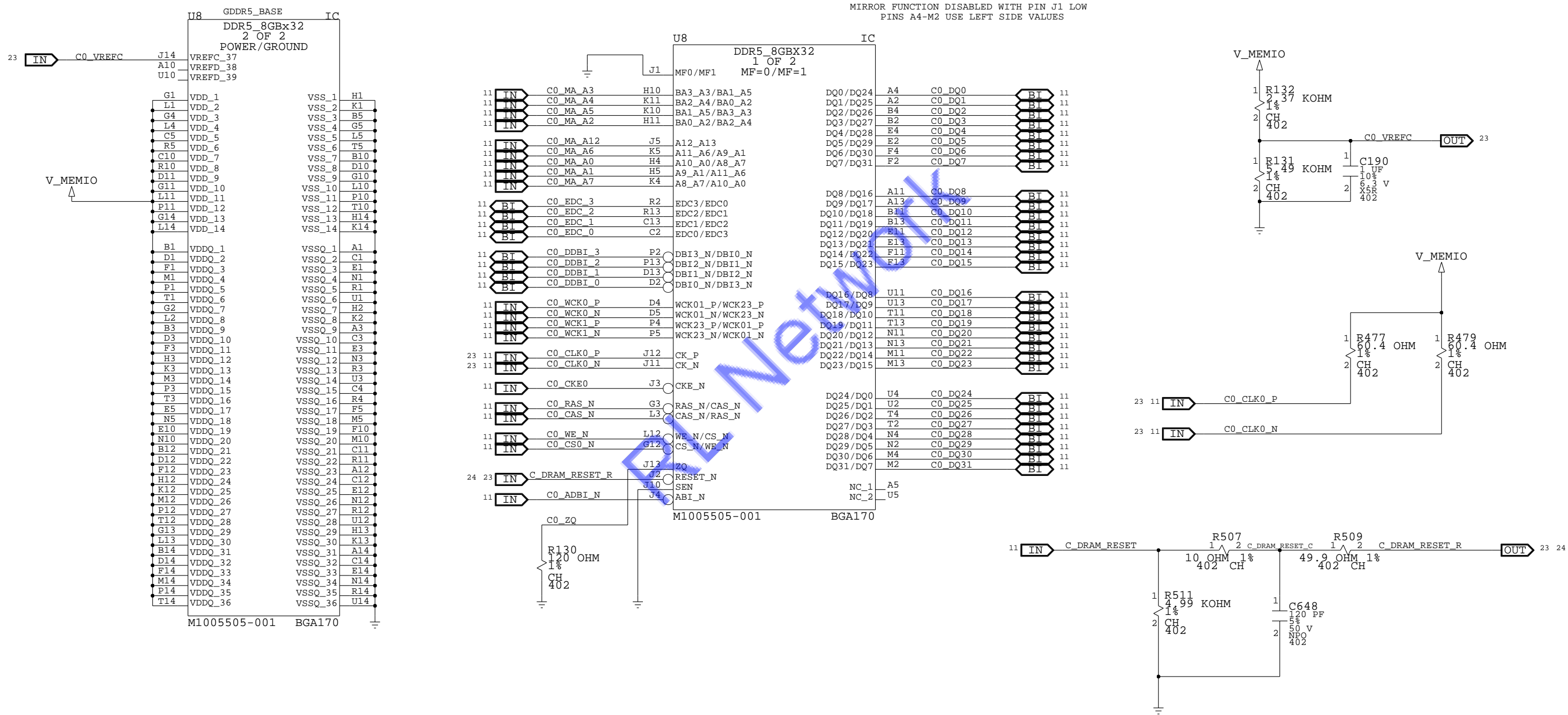
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FAB G-R

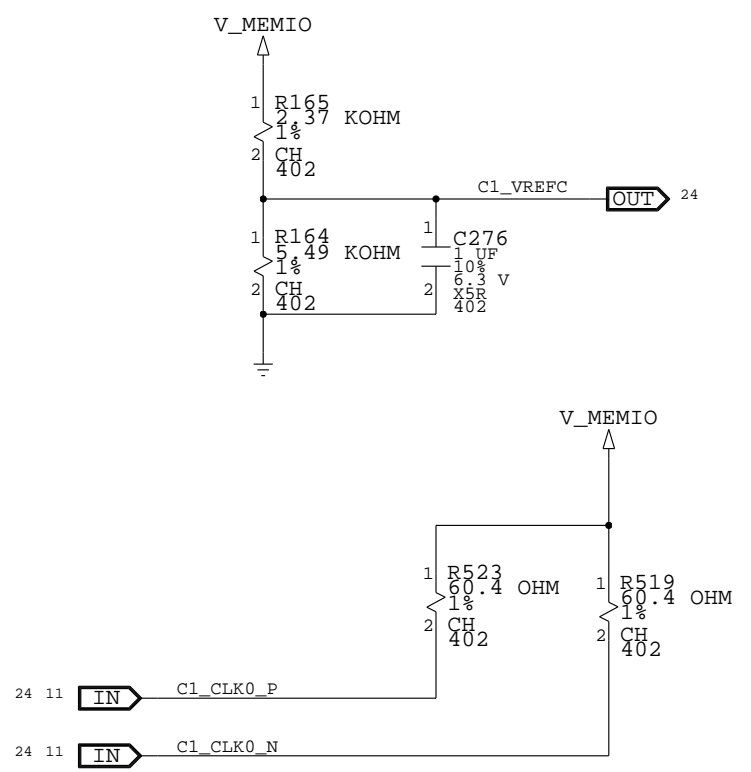
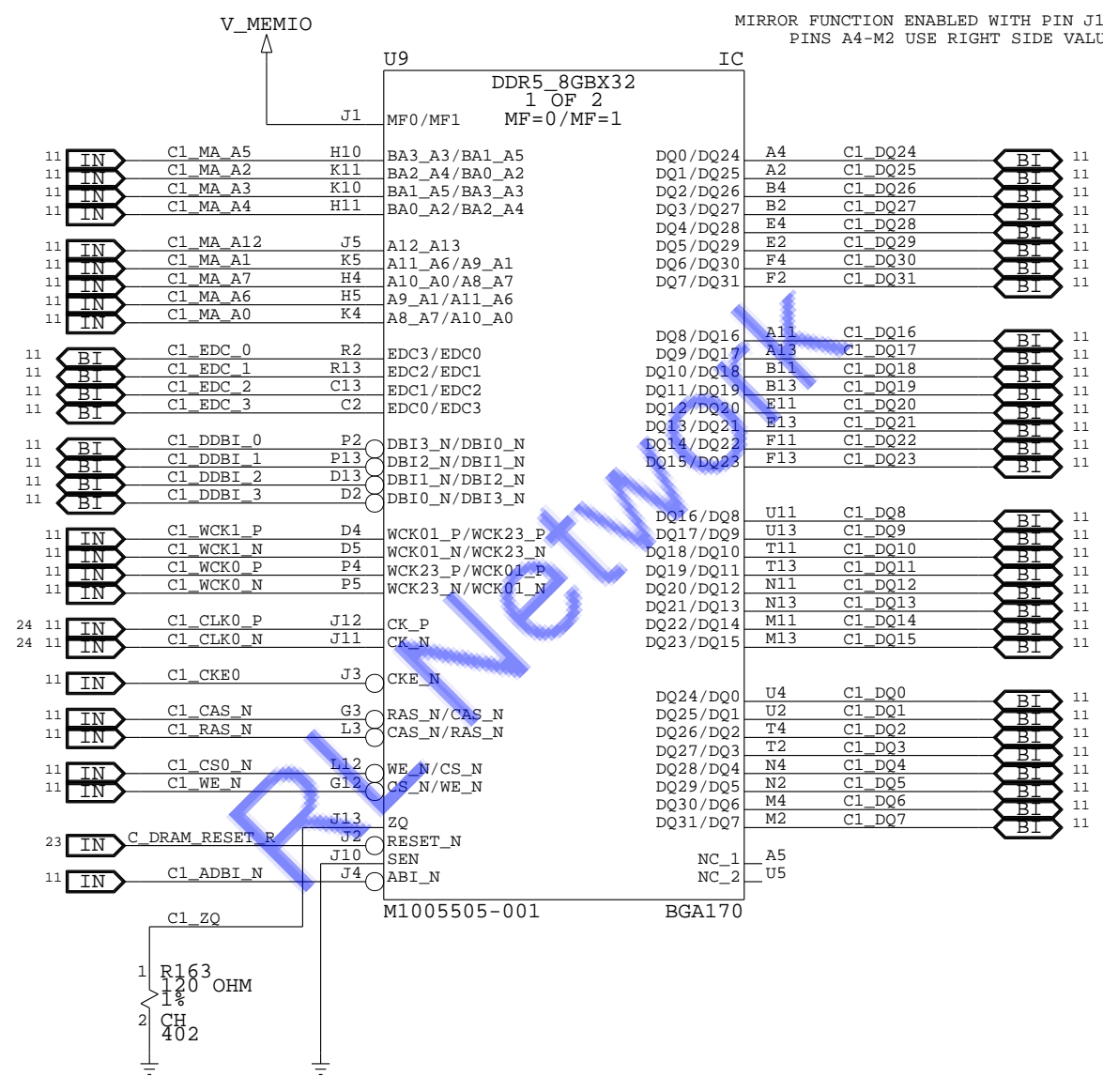
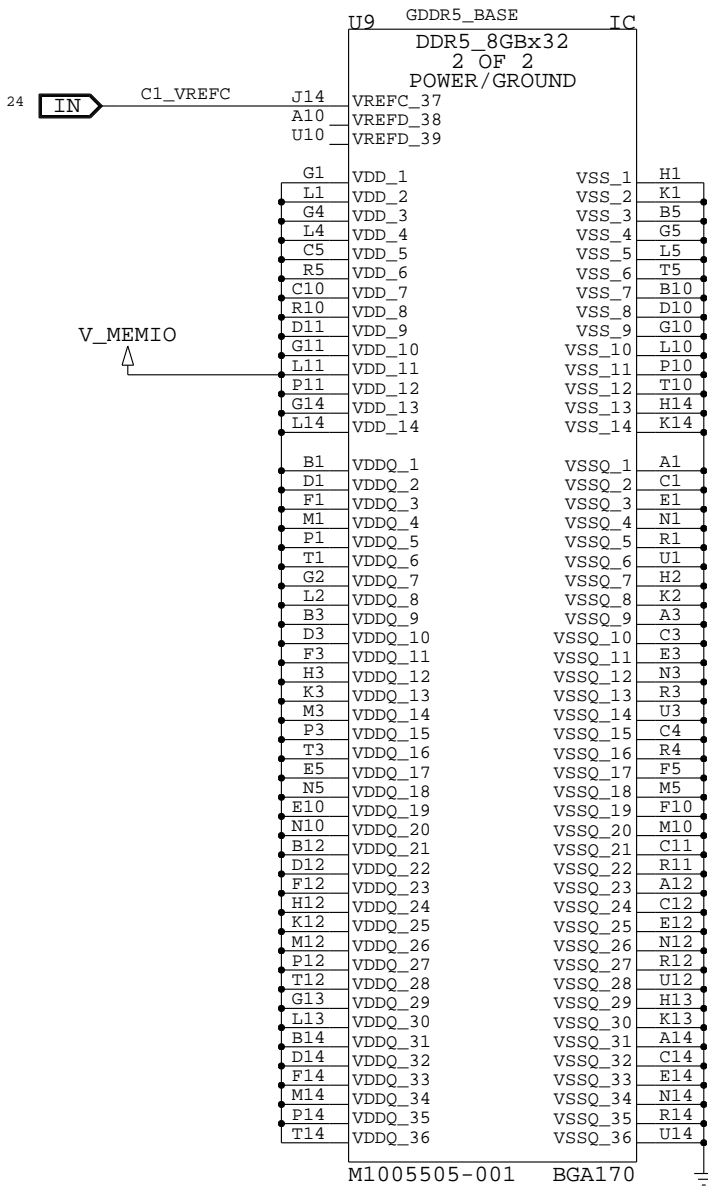
VER 0.991



MEMORY: CHANNEL C0

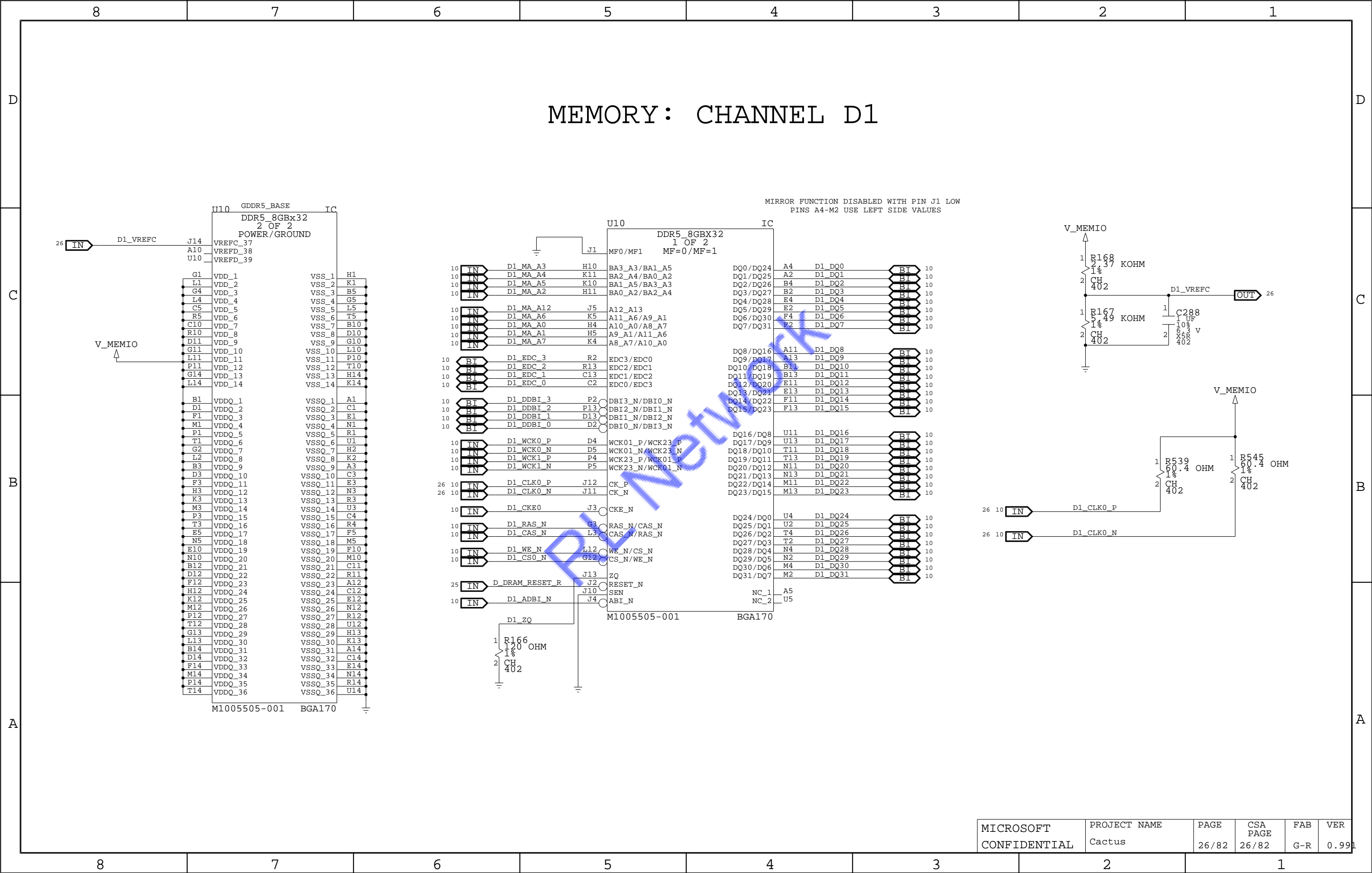


MEMORY: CHANNEL C1





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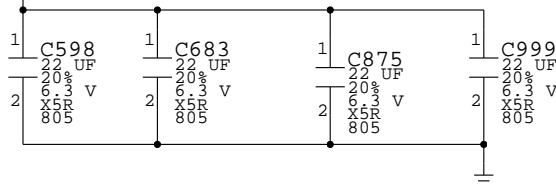
G-R

VER

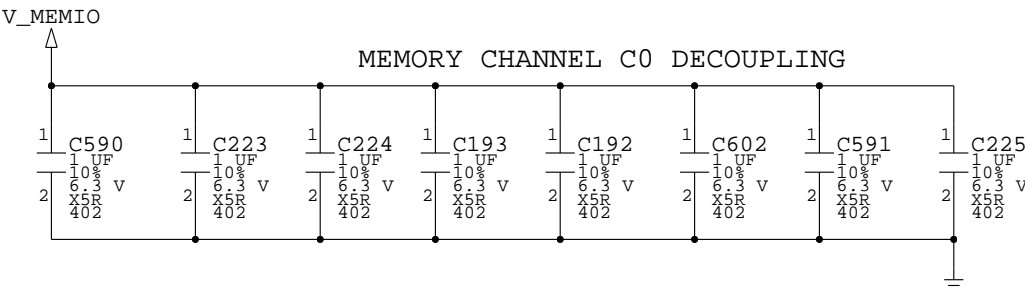
0.99

# MEMORY: CHANNEL C/D DECOUPLING

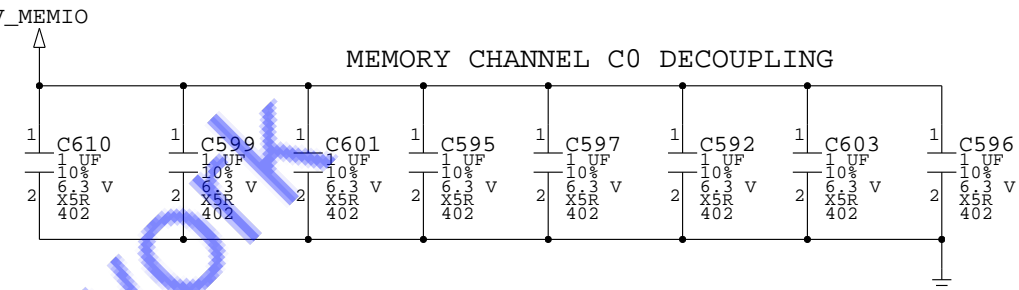
V\_MEMIO CHANNEL C/D DECOUPLING



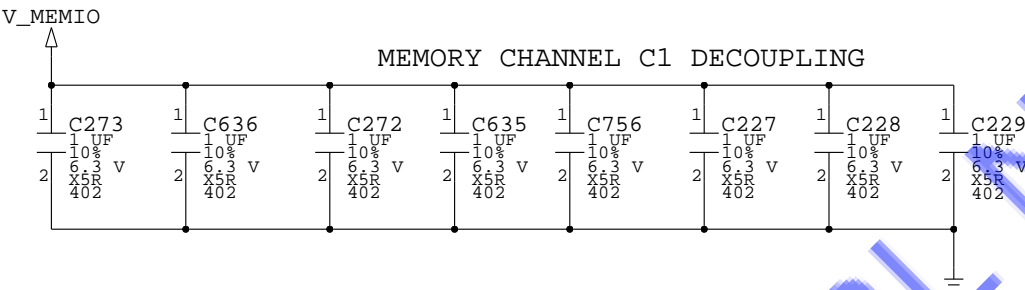
MEMORY CHANNEL C0 DECOUPLING



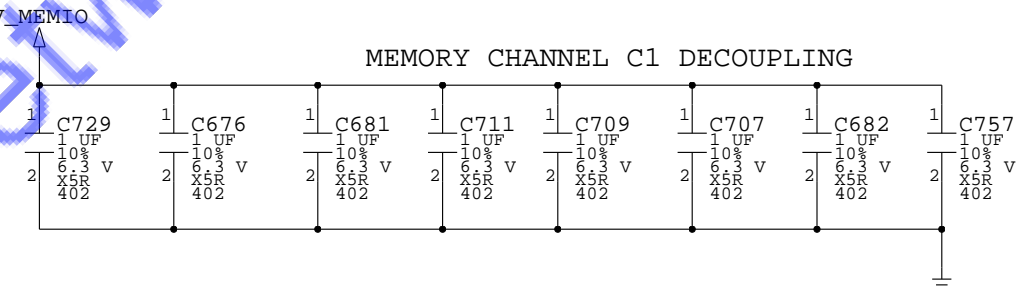
MEMORY CHANNEL C0 DECOUPLING



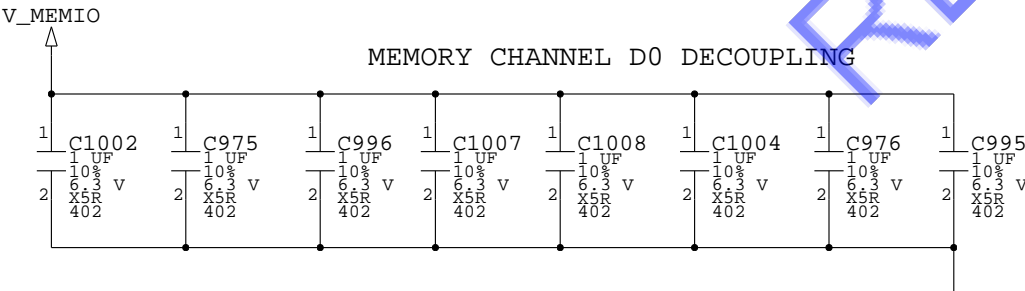
MEMORY CHANNEL C1 DECOUPLING



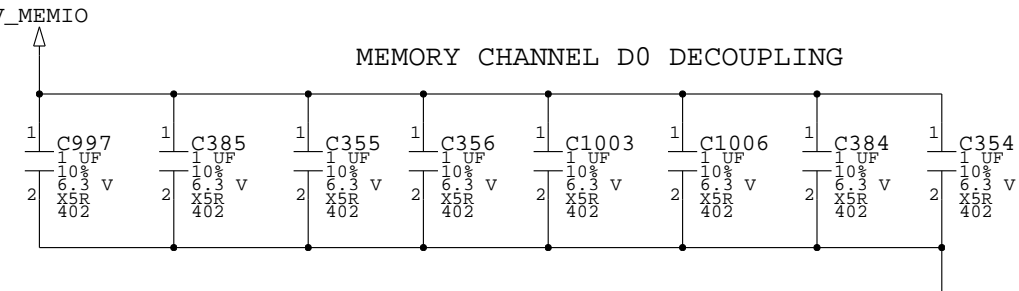
MEMORY CHANNEL C1 DECOUPLING



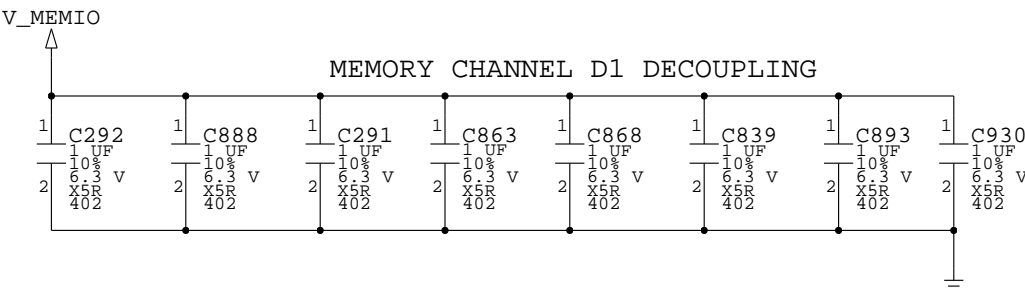
MEMORY CHANNEL D0 DECOUPLING



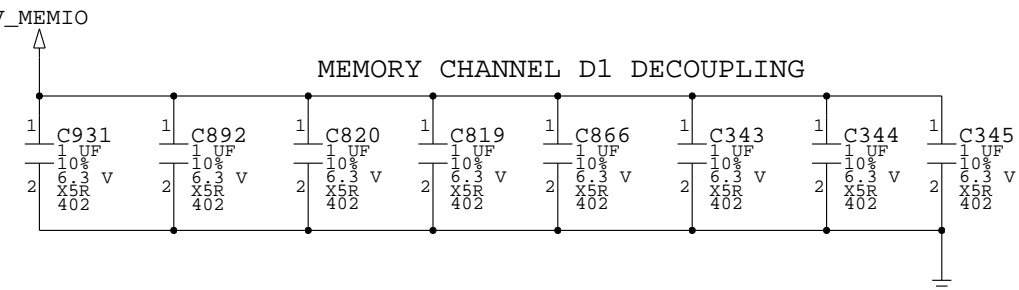
MEMORY CHANNEL D0 DECOUPLING



MEMORY CHANNEL D1 DECOUPLING



MEMORY CHANNEL D1 DECOUPLING



NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

## T





[illegible]

**MEMORY: CHANNEL F0**

MIRROR FUNCTION DISABLED WITH PIN J1 LOW  
PINS A4-M2 USE LEFT SIDE VALUES

**U14: DDR5\_8GBx32 1 OF 2**  
MF0/MF1 MF=0/MF=1

**U10: GDDR5\_BASE IC**  
DDR5\_8GBx32 2 OF 2  
POWER/GROUND

**M1005505-001 BGA170**

**Signal Connections:**

- Power/Ground:** VDD\_1 to VDD\_36, VSS\_1 to VSS\_36, VSSQ\_1 to VSSQ\_36.
- Data Bus:** DQ0/DQ24 to DQ31/DQ7, DQ8/DQ16 to DQ15/DQ23, DQ16/DQ8 to DQ17/DQ9, DQ17/DQ9 to DQ18/DQ10, DQ18/DQ10 to DQ19/DQ11, DQ19/DQ11 to DQ20/DQ12, DQ20/DQ12 to DQ21/DQ13, DQ21/DQ13 to DQ22/DQ14, DQ22/DQ14 to DQ23/DQ15, DQ24/DQ0 to U4 F0\_DQ24, DQ25/DQ1 to U2 F0\_DQ25, DQ26/DQ2 to T4 F0\_DQ26, DQ27/DQ3 to T2 F0\_DQ27, DQ28/DQ4 to N4 F0\_DQ28, DQ29/DQ5 to N2 F0\_DQ29, DQ30/DQ6 to M4 F0\_DQ30, DQ31/DQ7 to M2 F0\_DQ31.
- Control Signals:** F0\_MA\_A3 to F0\_MA\_A7, F0\_MA\_A12 to F0\_MA\_A7, F0\_EDC\_3 to F0\_EDC\_0, F0\_DDBI\_3 to F0\_DDBI\_0, F0\_WCK0\_P to F0\_WCK1\_N, F0\_CLK0\_P to F0\_CLK0\_N, F0\_CKE0, F0\_RAS\_N, F0\_CAS\_N, F0\_WE\_N, F0\_CS0\_N, F0\_DRAM\_RESET\_R, F0\_ADBI\_N, F0\_ZQ.

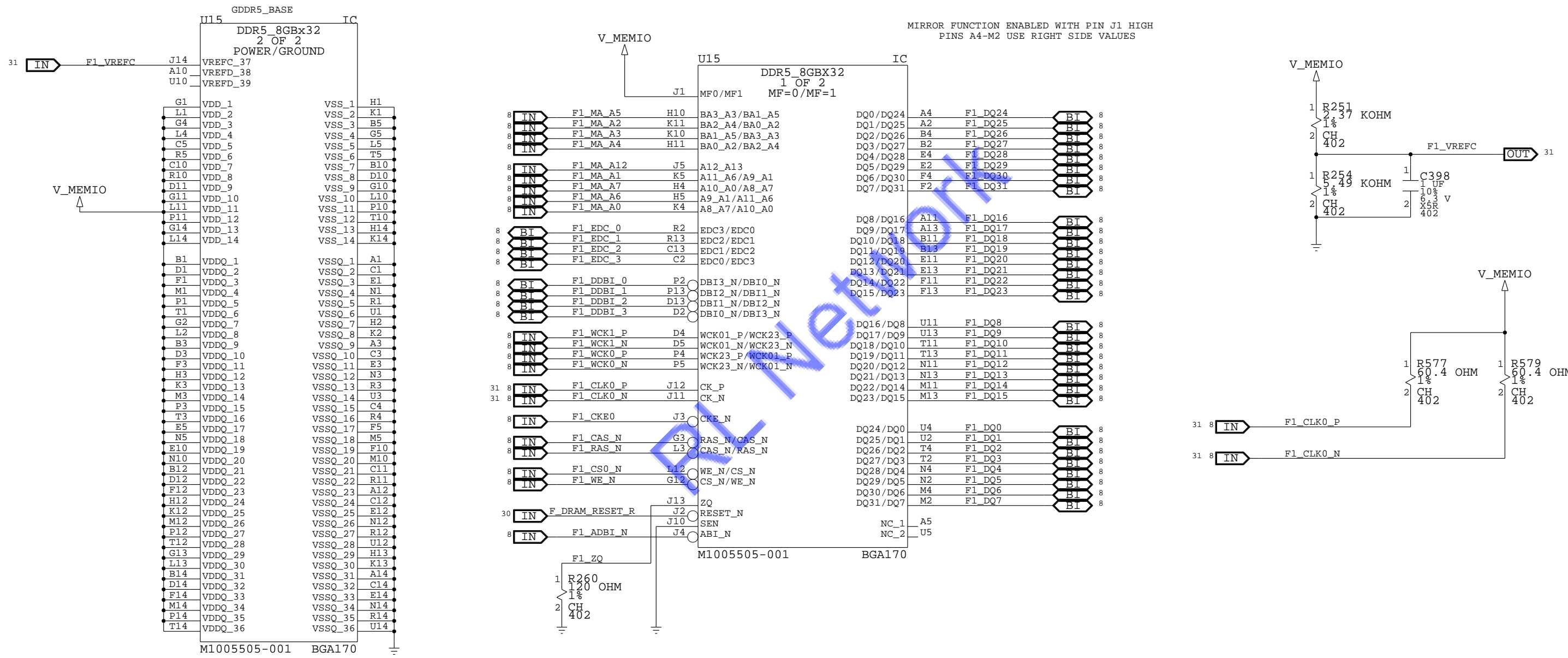
**Component Values:**

- Resistors:** R582, R584, R578, R576, R566, R567, R571.
- Capacitors:** C1046, C1015.
- Inductors:** L103, L103.
- Diodes:** D103, D103.

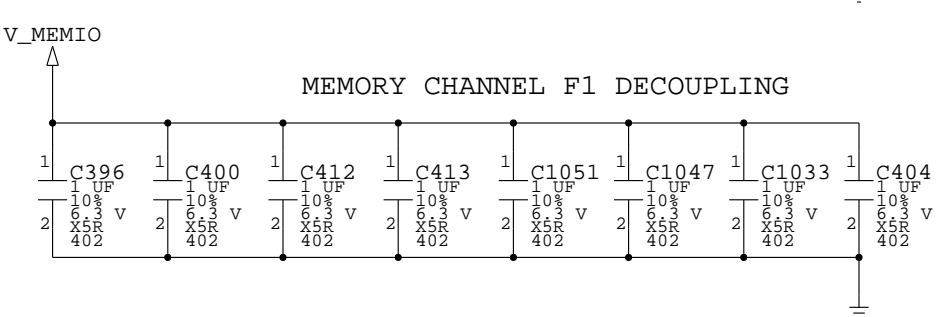
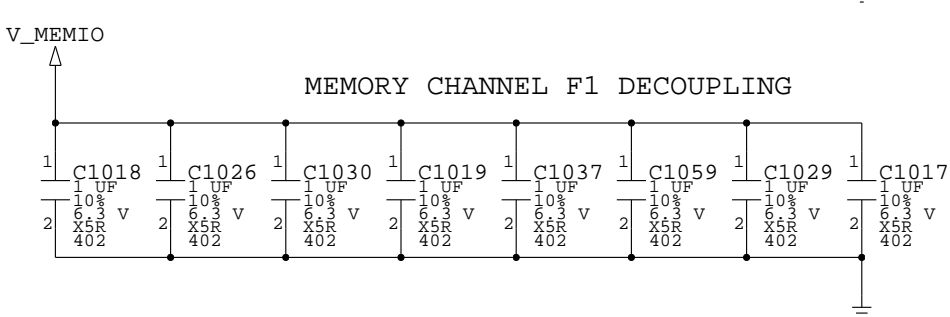
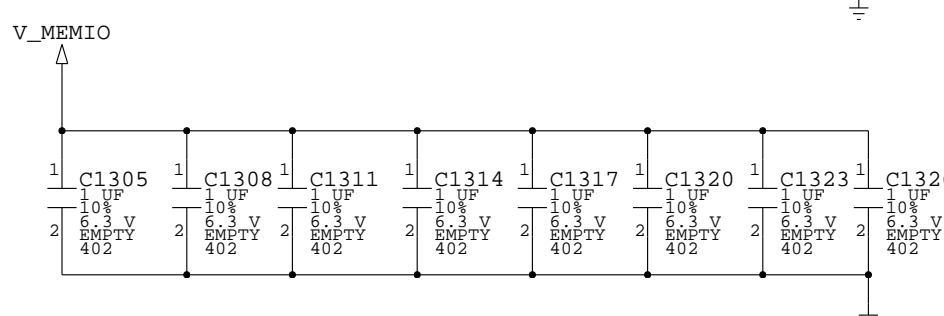
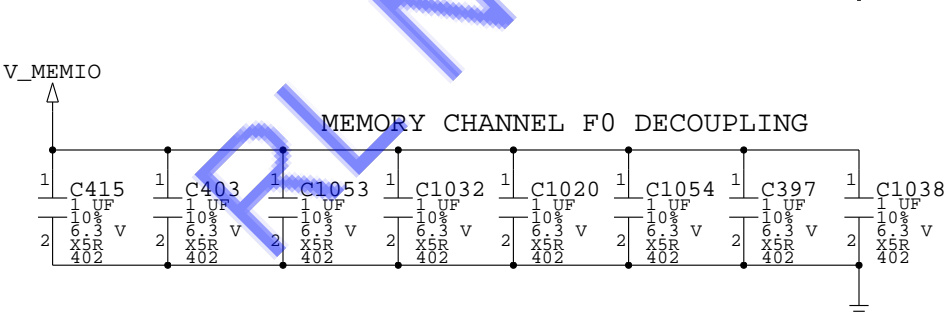
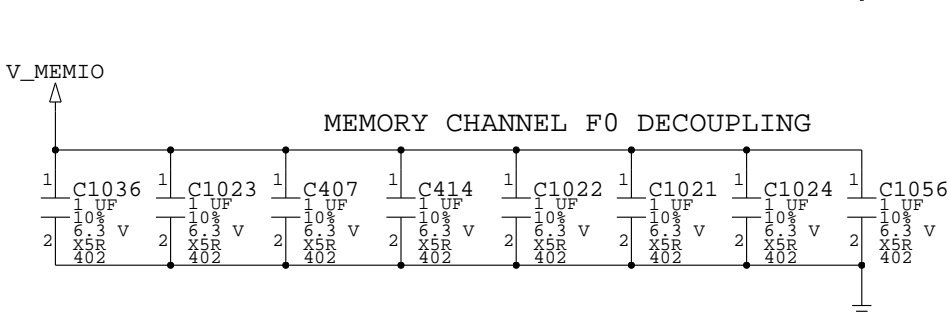
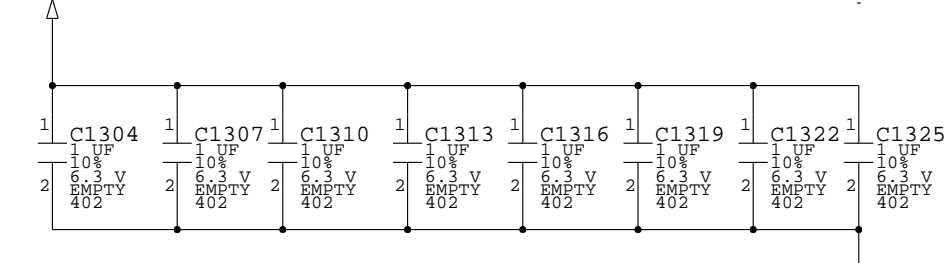
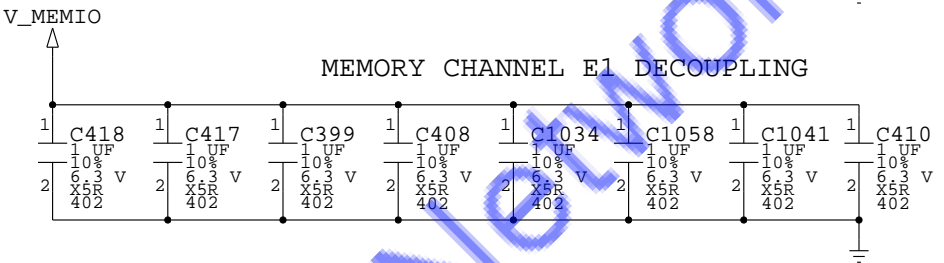
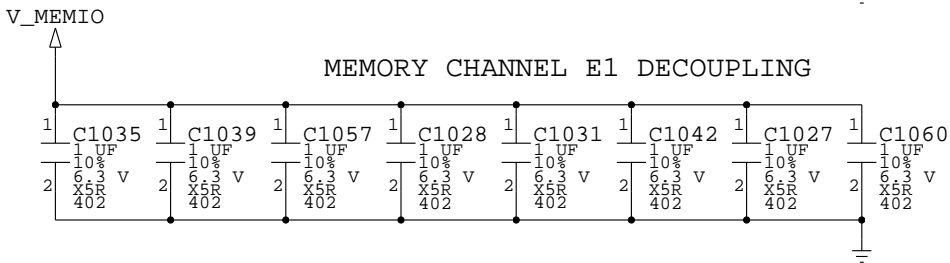
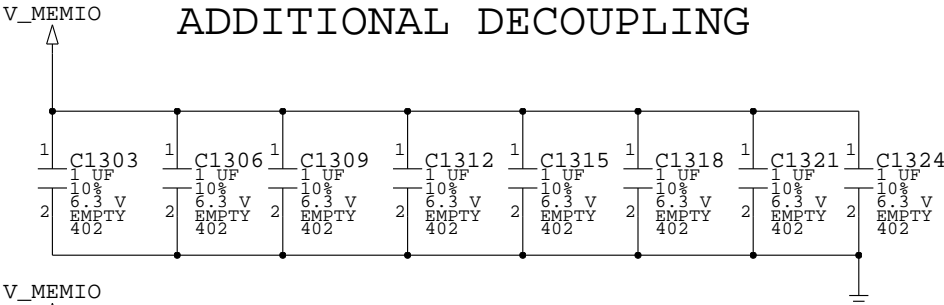
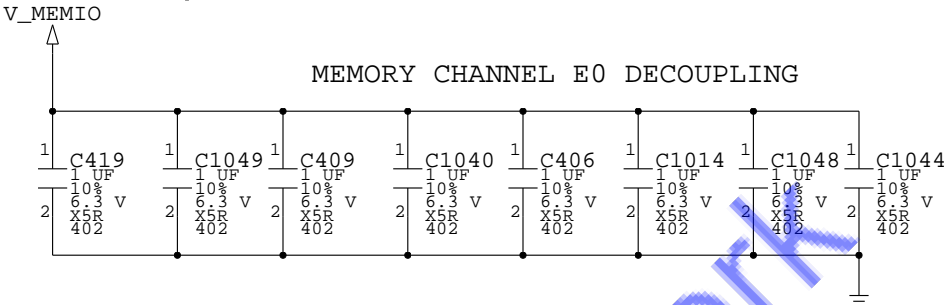
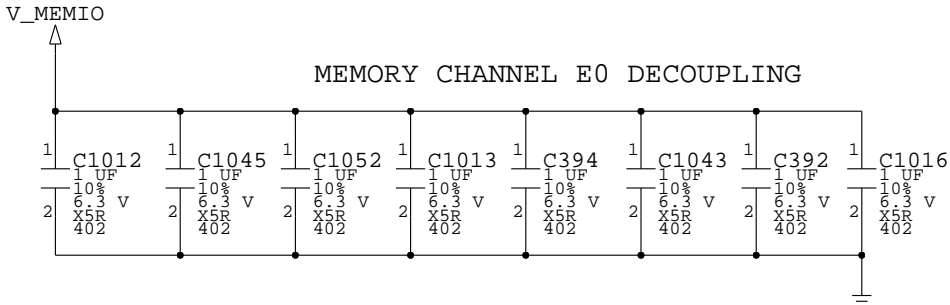
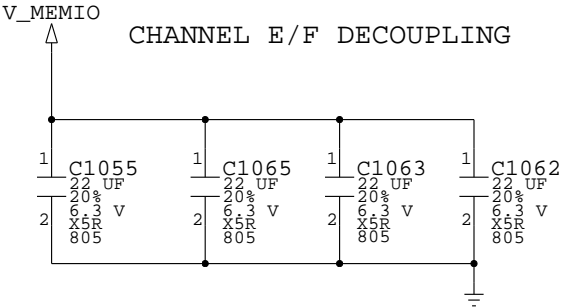
**Microcontroller Information:**

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MEMORY: CHANNEL F1



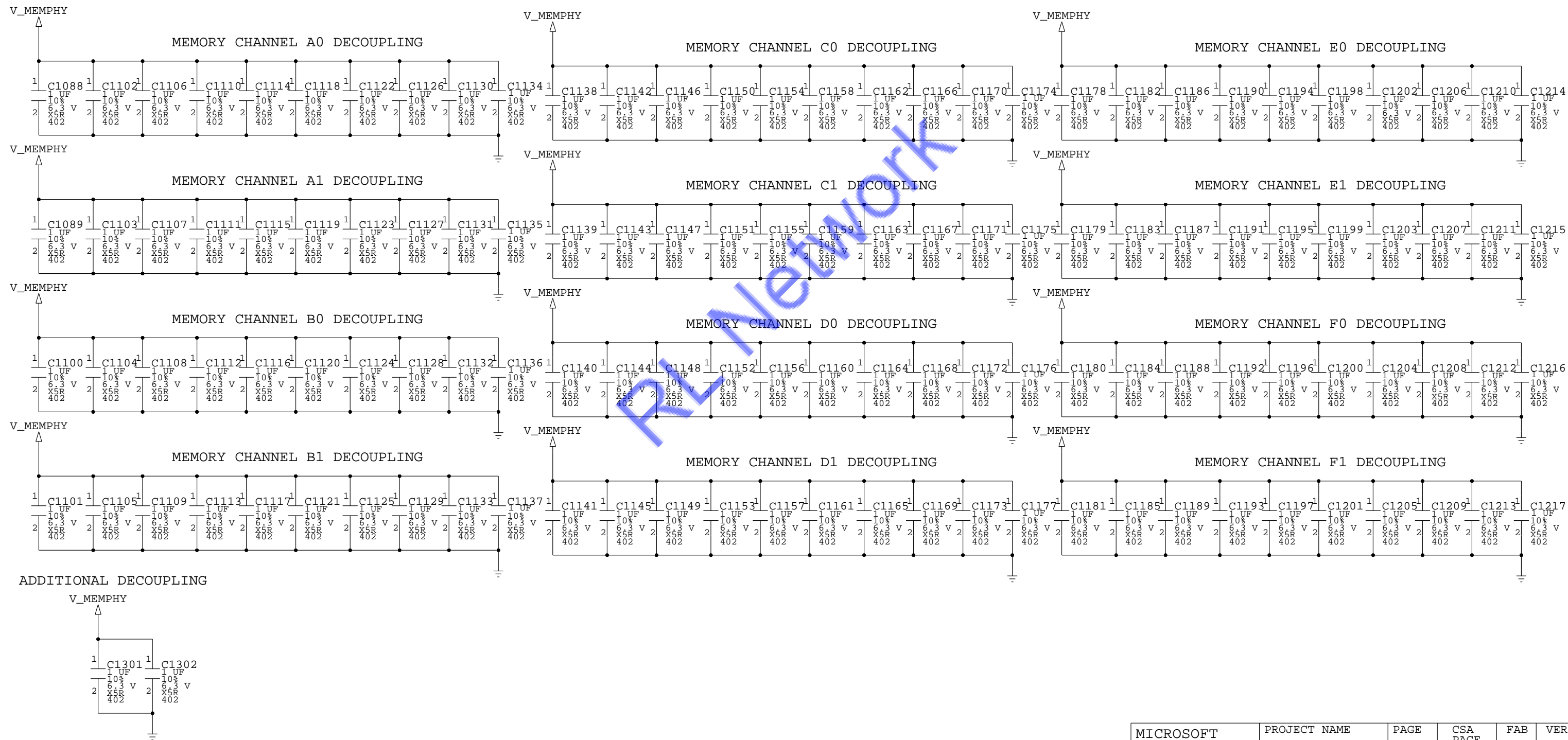
MEMORY: CHANNEL E/F DECOUPLING

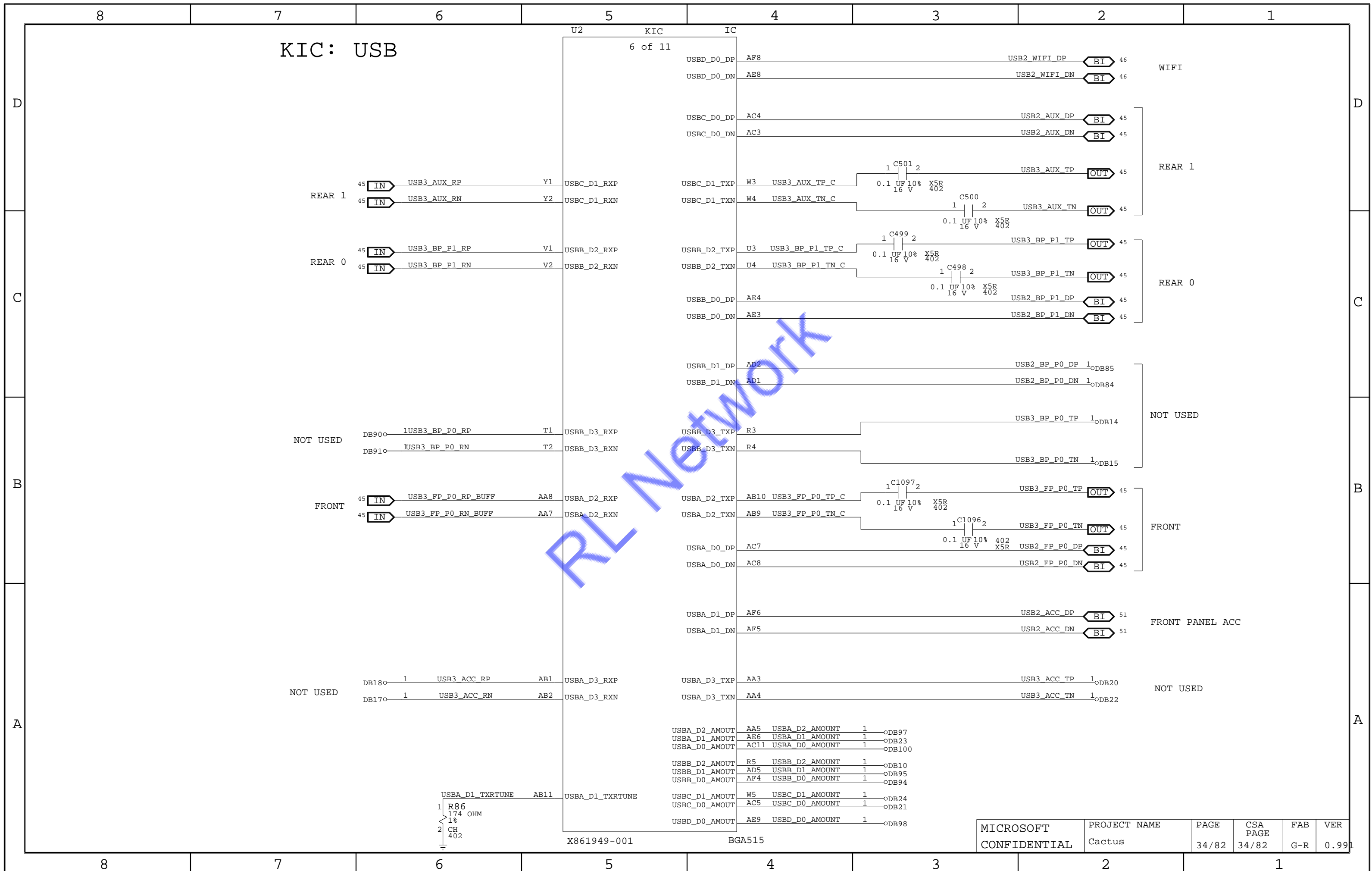


NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

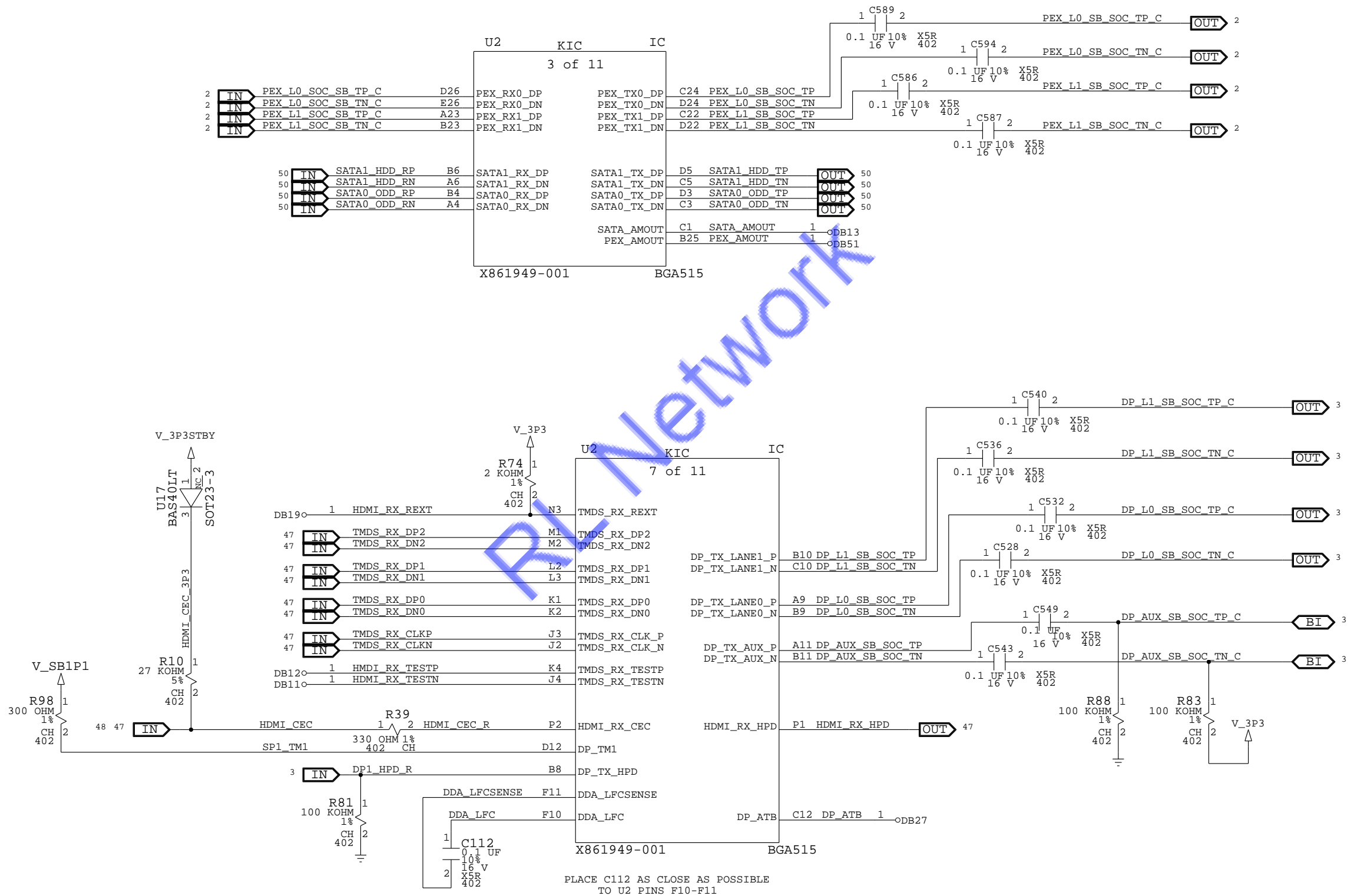


# MEMORY: ADDITIONAL DECOUPLING

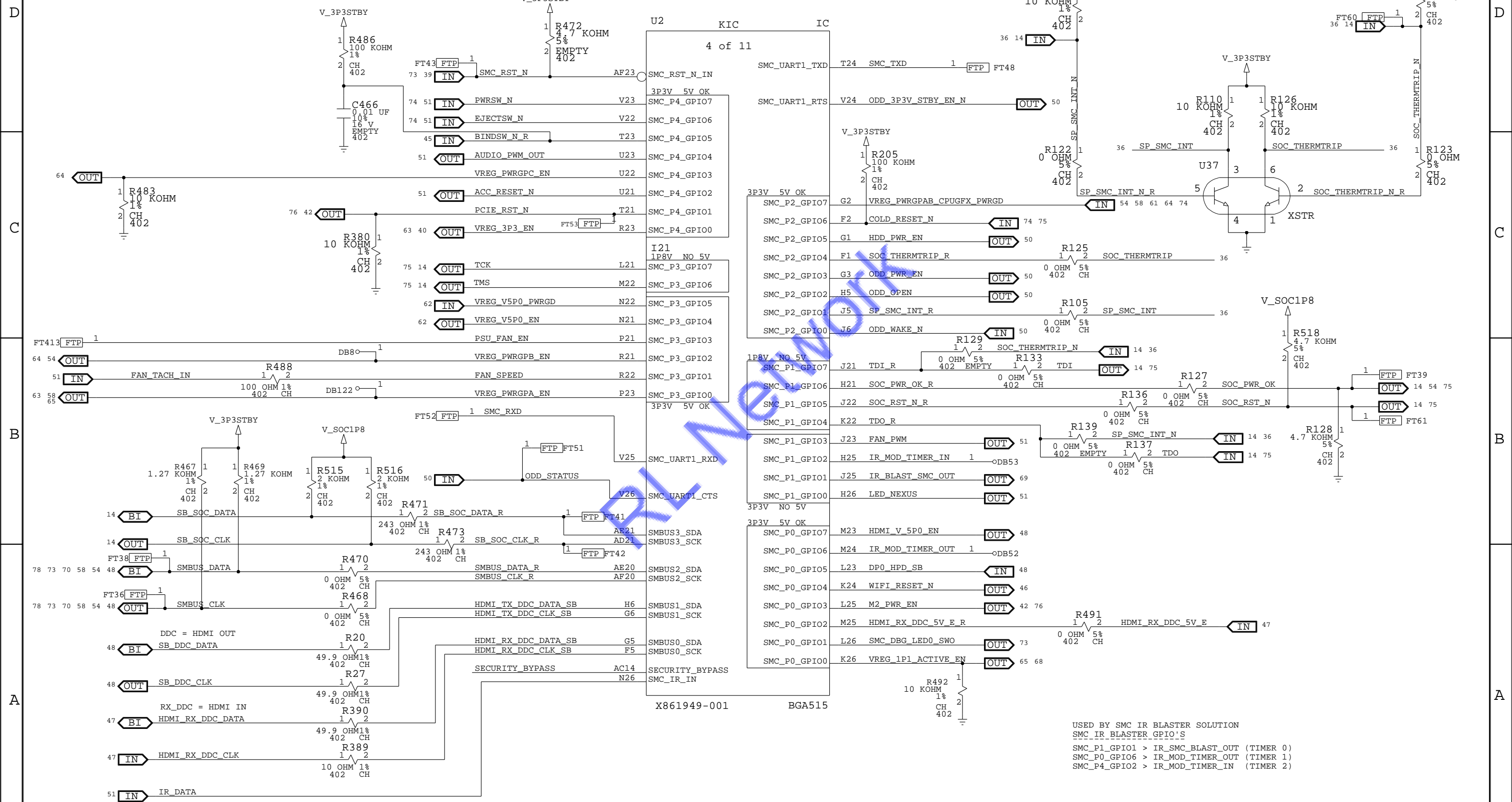




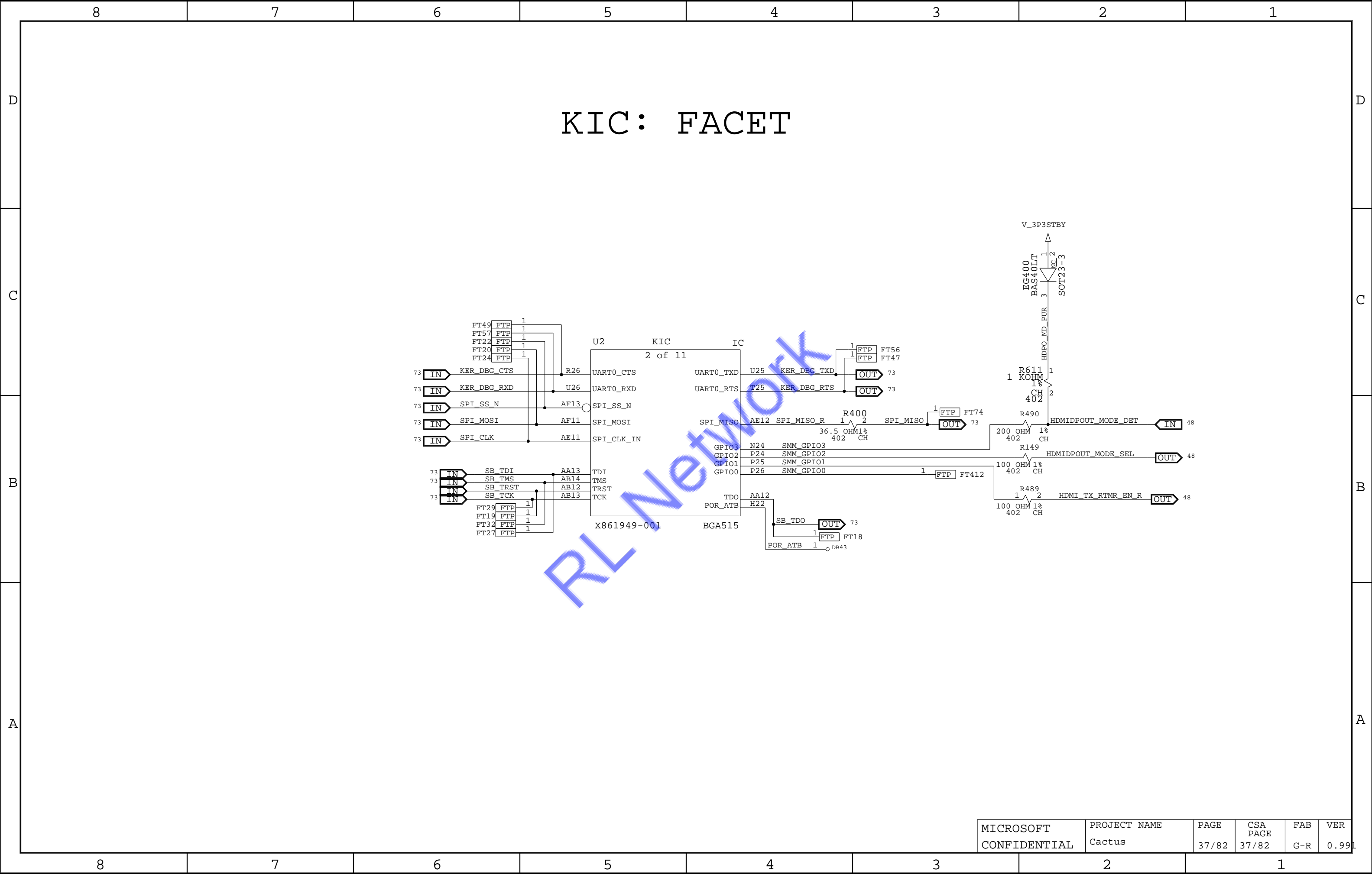
KIC: PCIEX, SATA, VIDEO



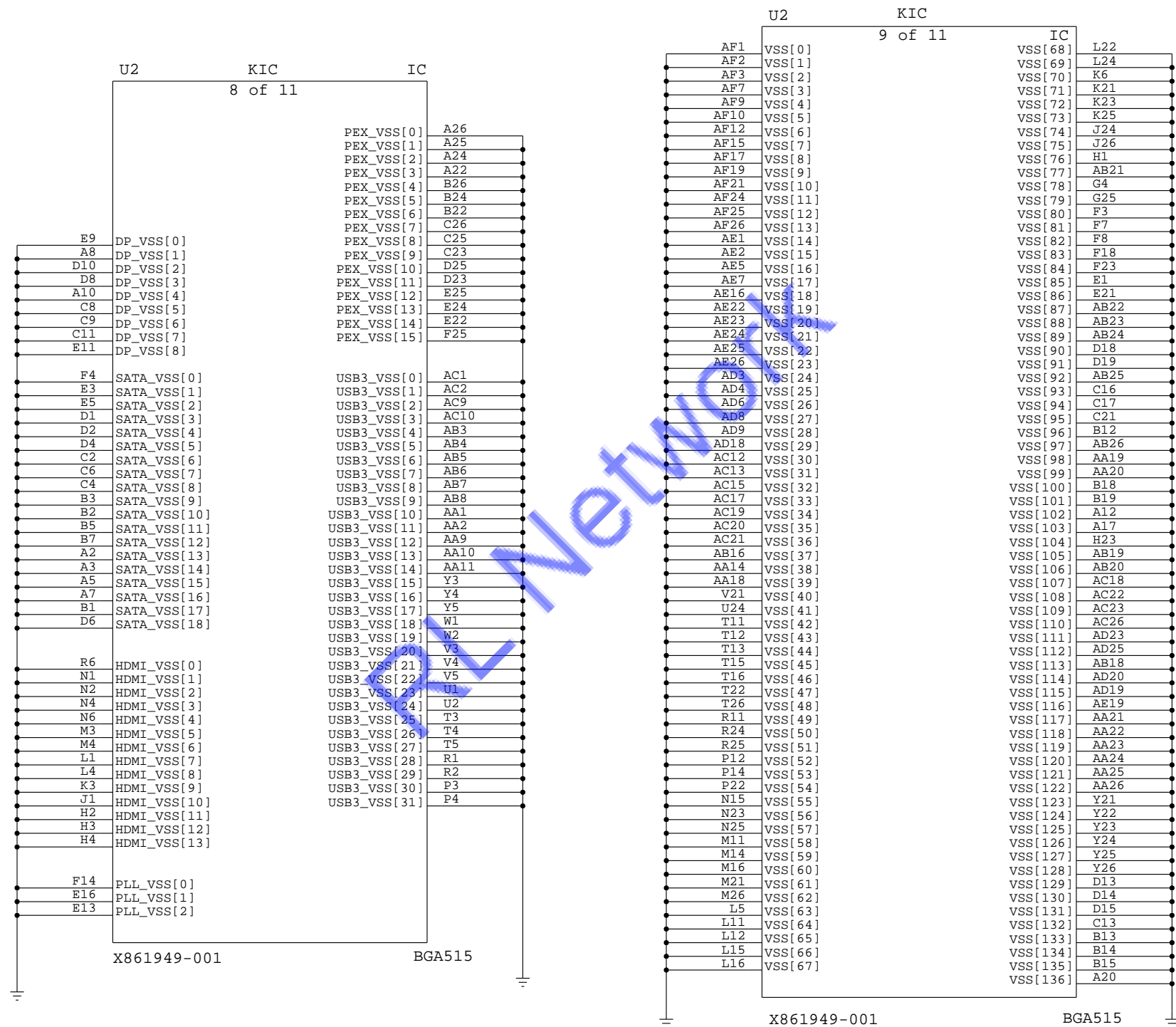
KIC: SMC

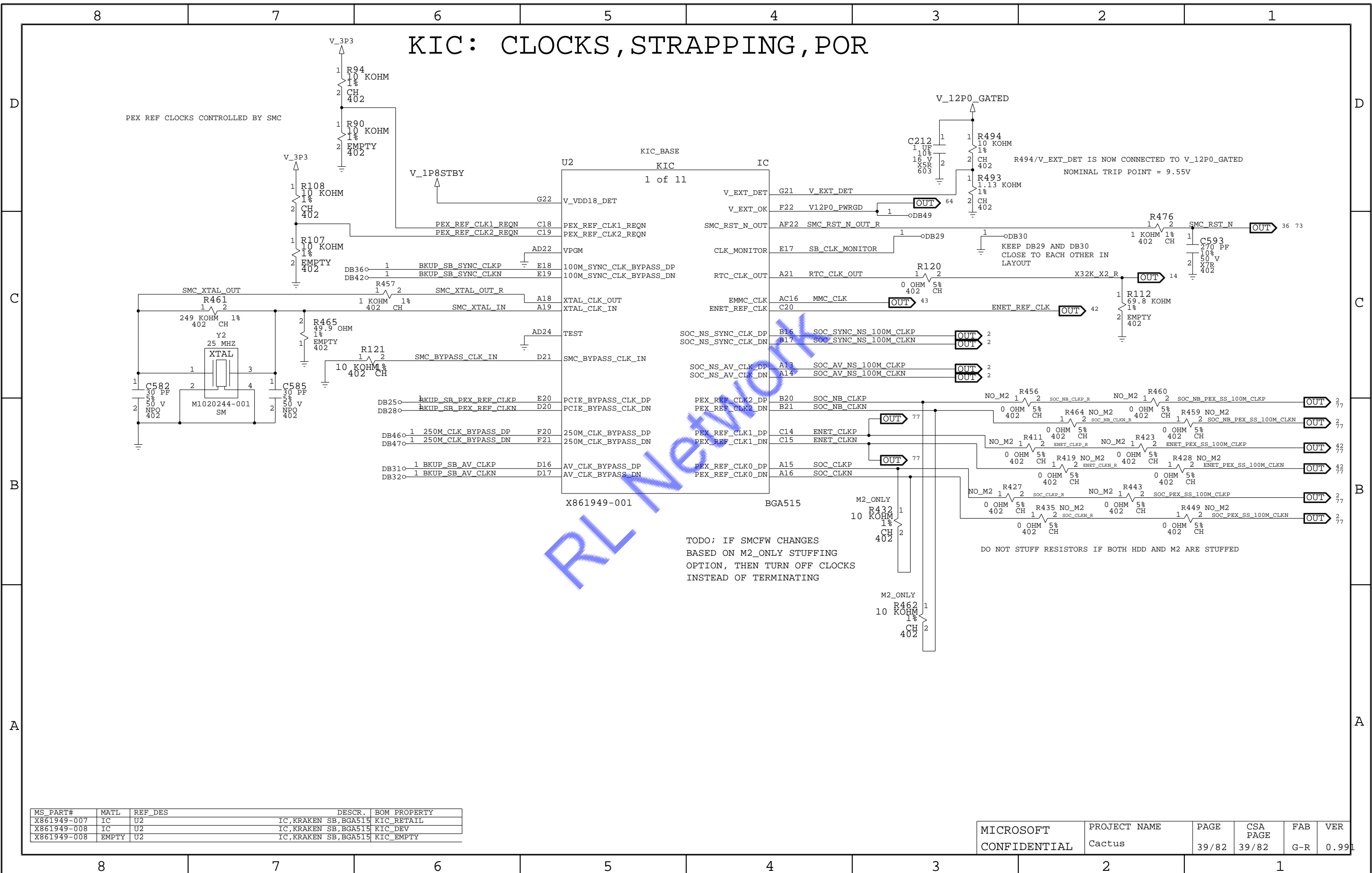






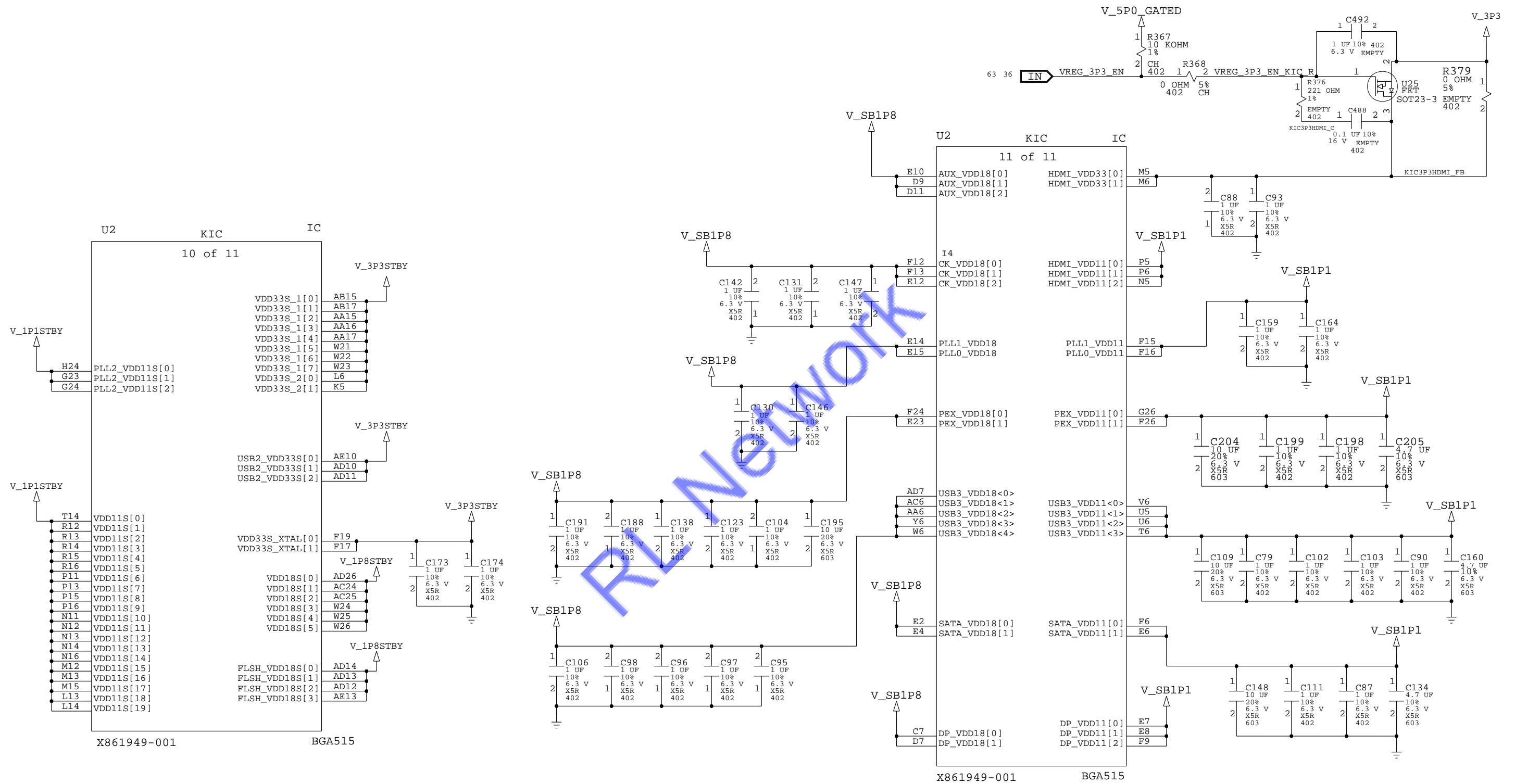
# KIC: POWER





KIC: POWER

FET PREVENTS LEAKAGE THROUGH KRAKEN  
FROM STANDBY RAILS TO 3P3 RAIL



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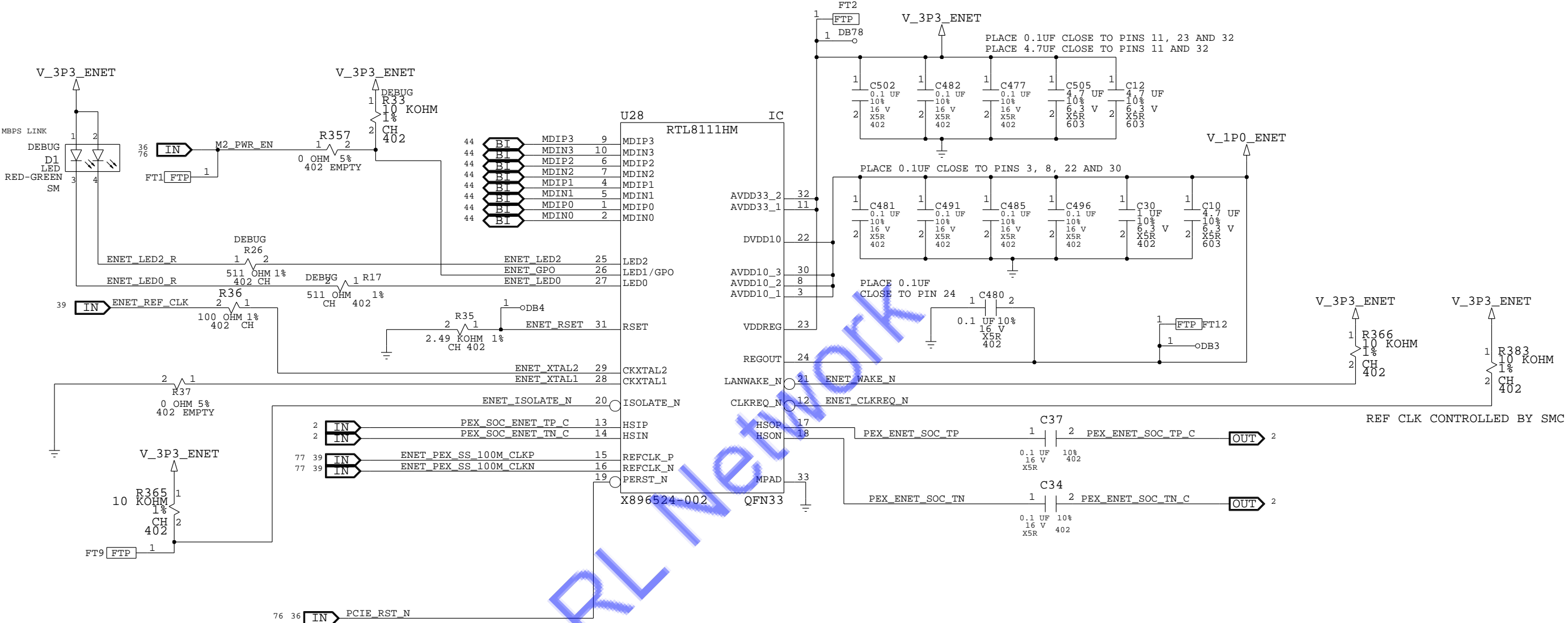
## D



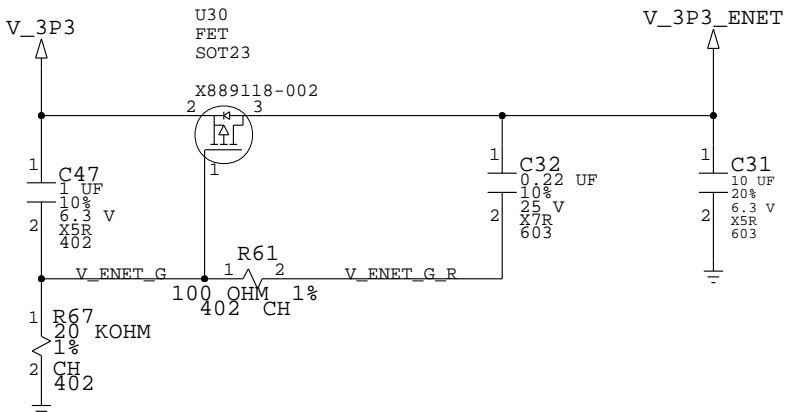
MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 41/82	CSA PAGE 41/82	FAB G-R	VER 0.991
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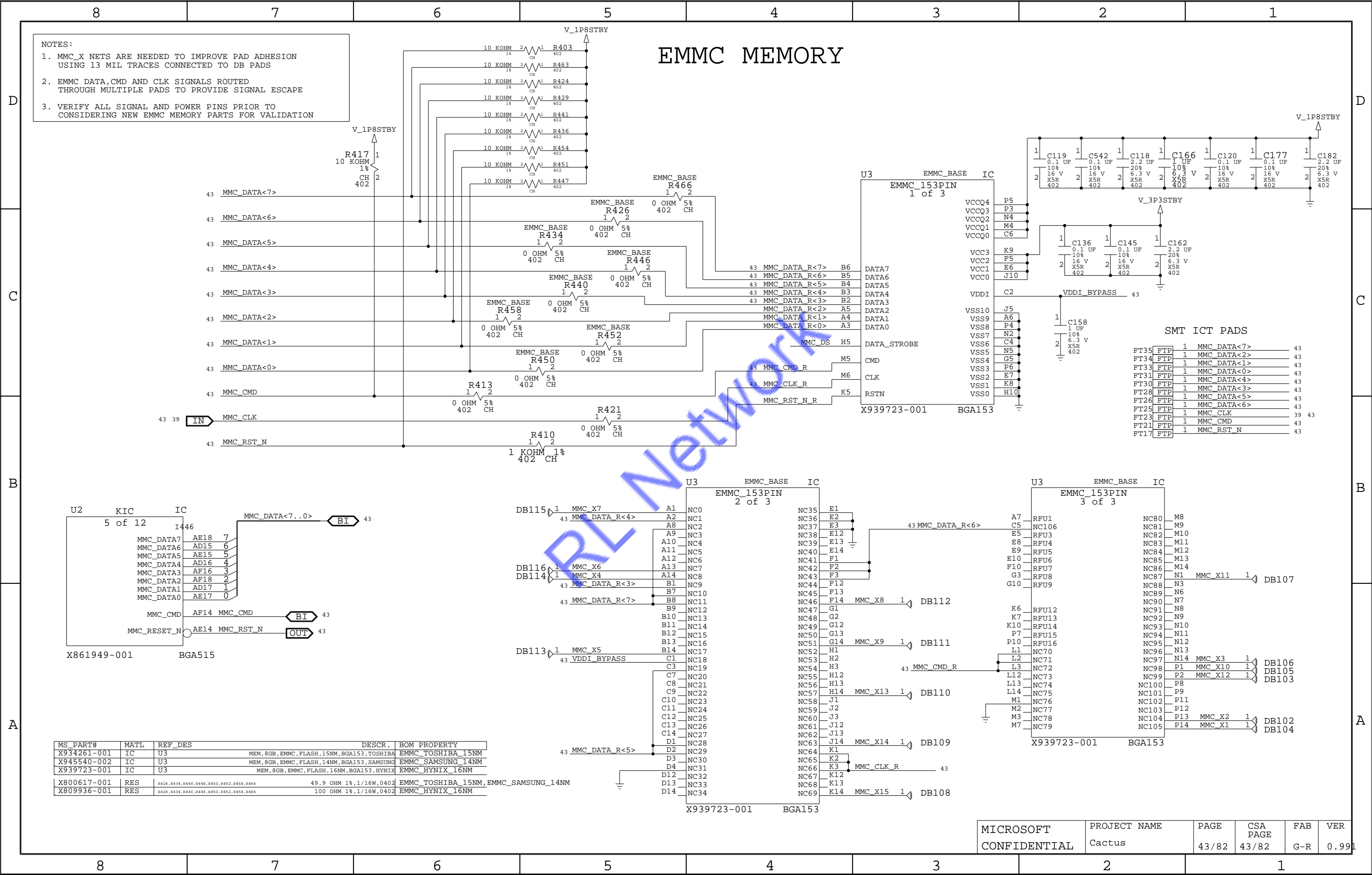


ETHERNET CONTROLLER

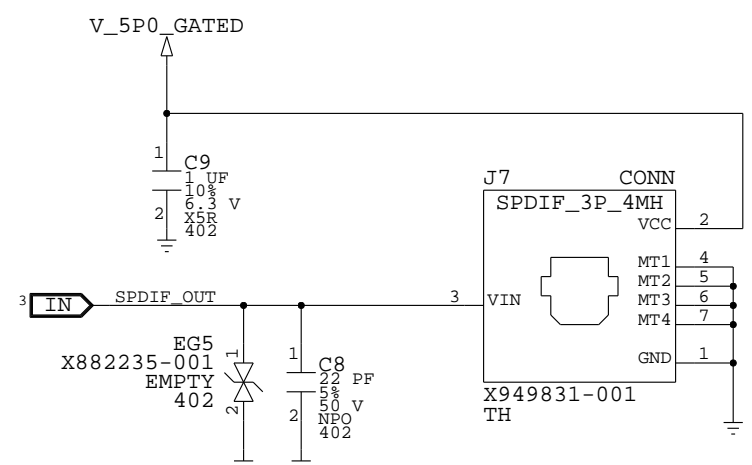
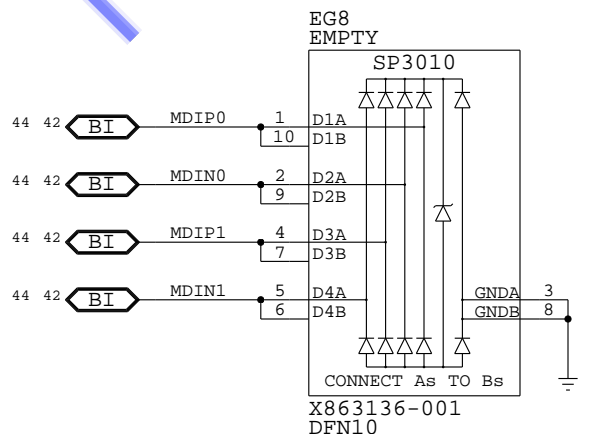
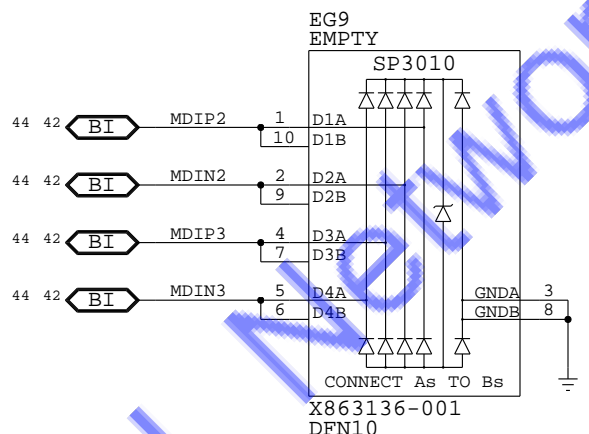
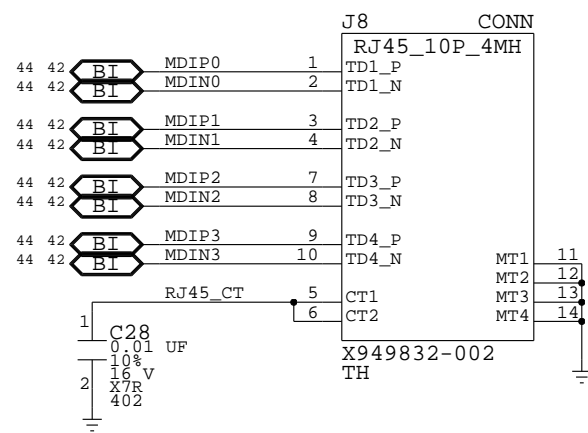


SOFT START  
NOM. VOLTAGE: 3.3V  
MAX POWER: 590MW

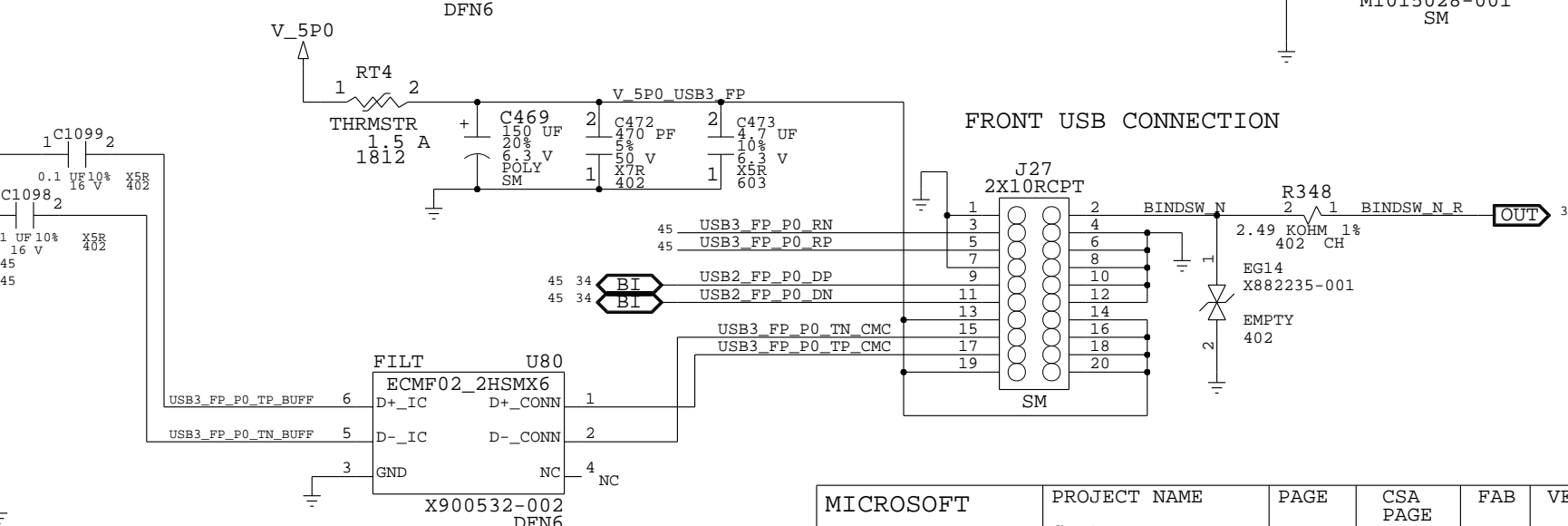
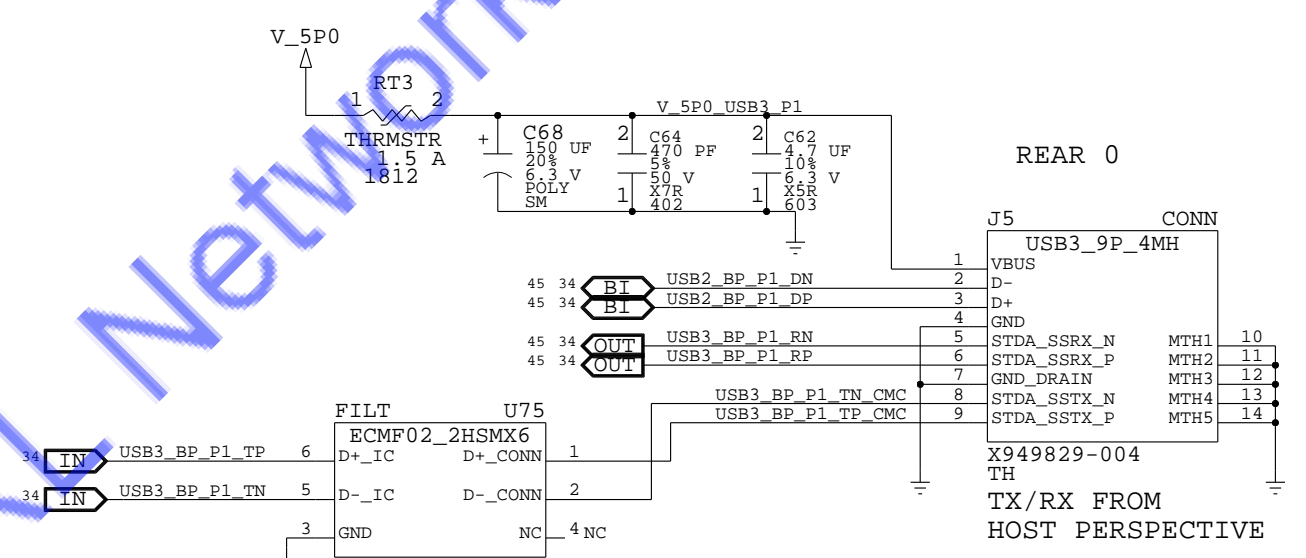
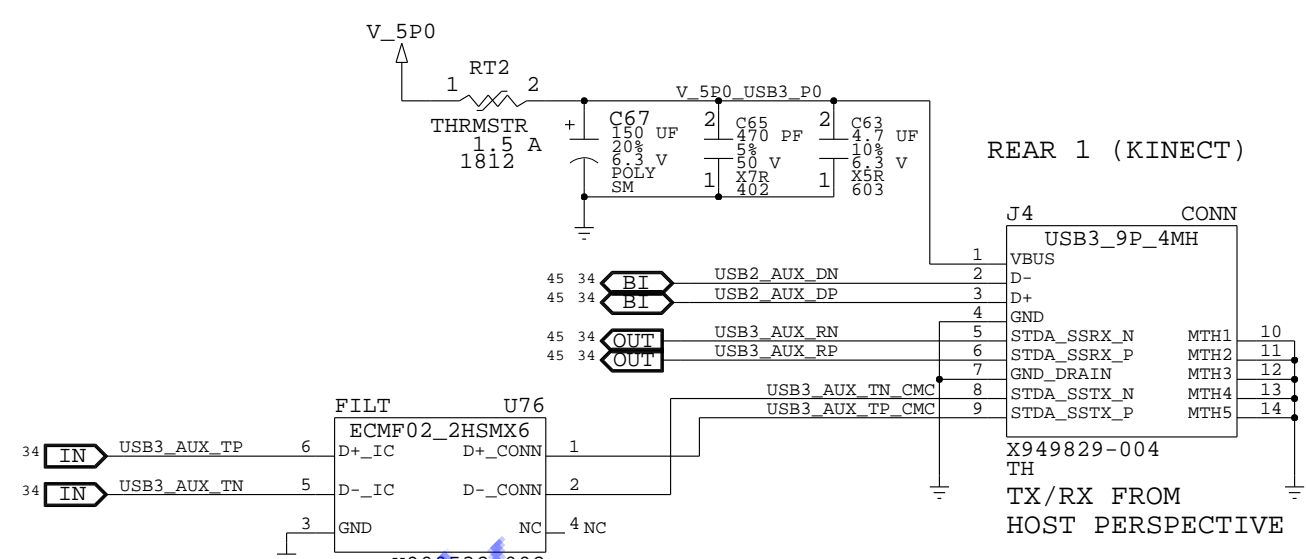
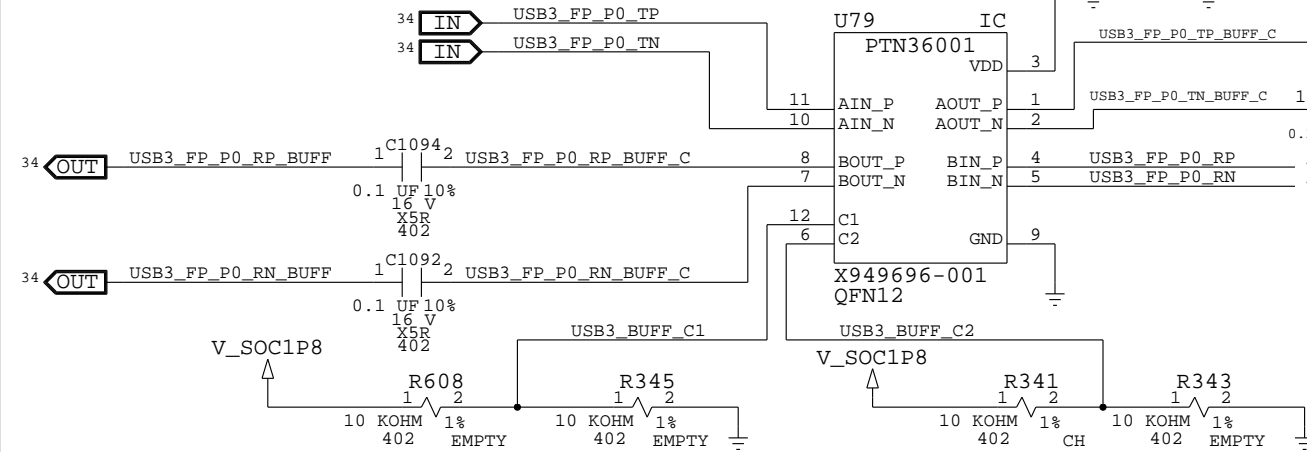
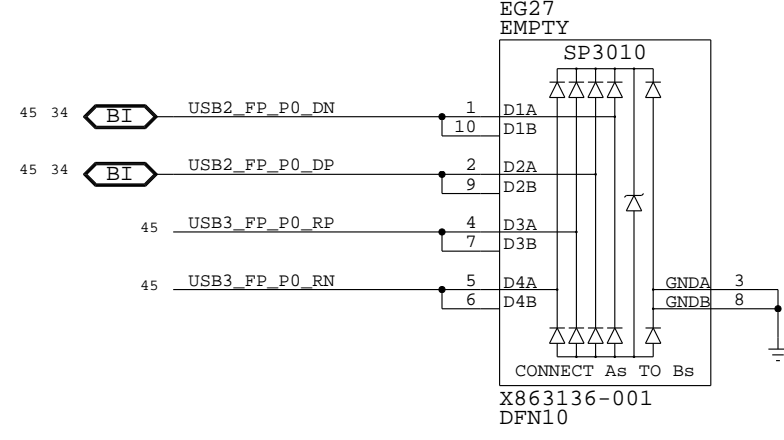
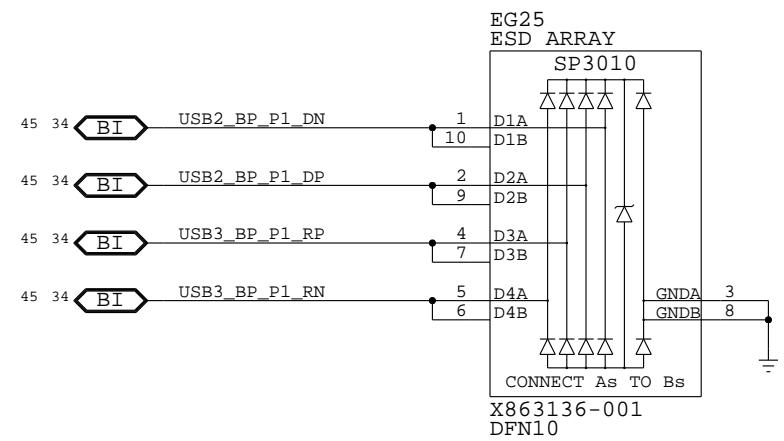
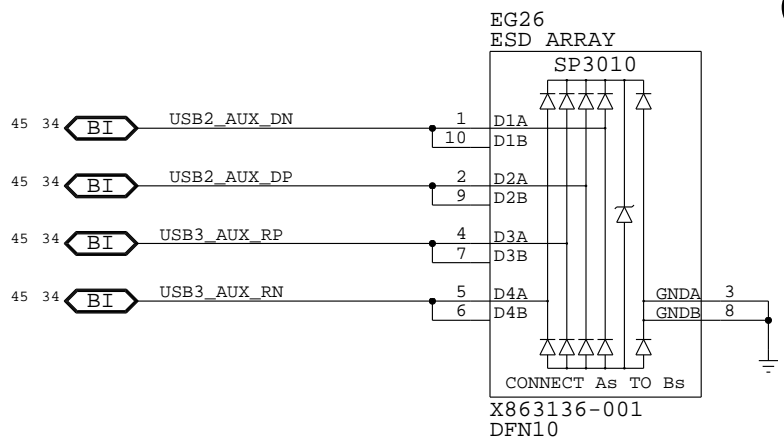


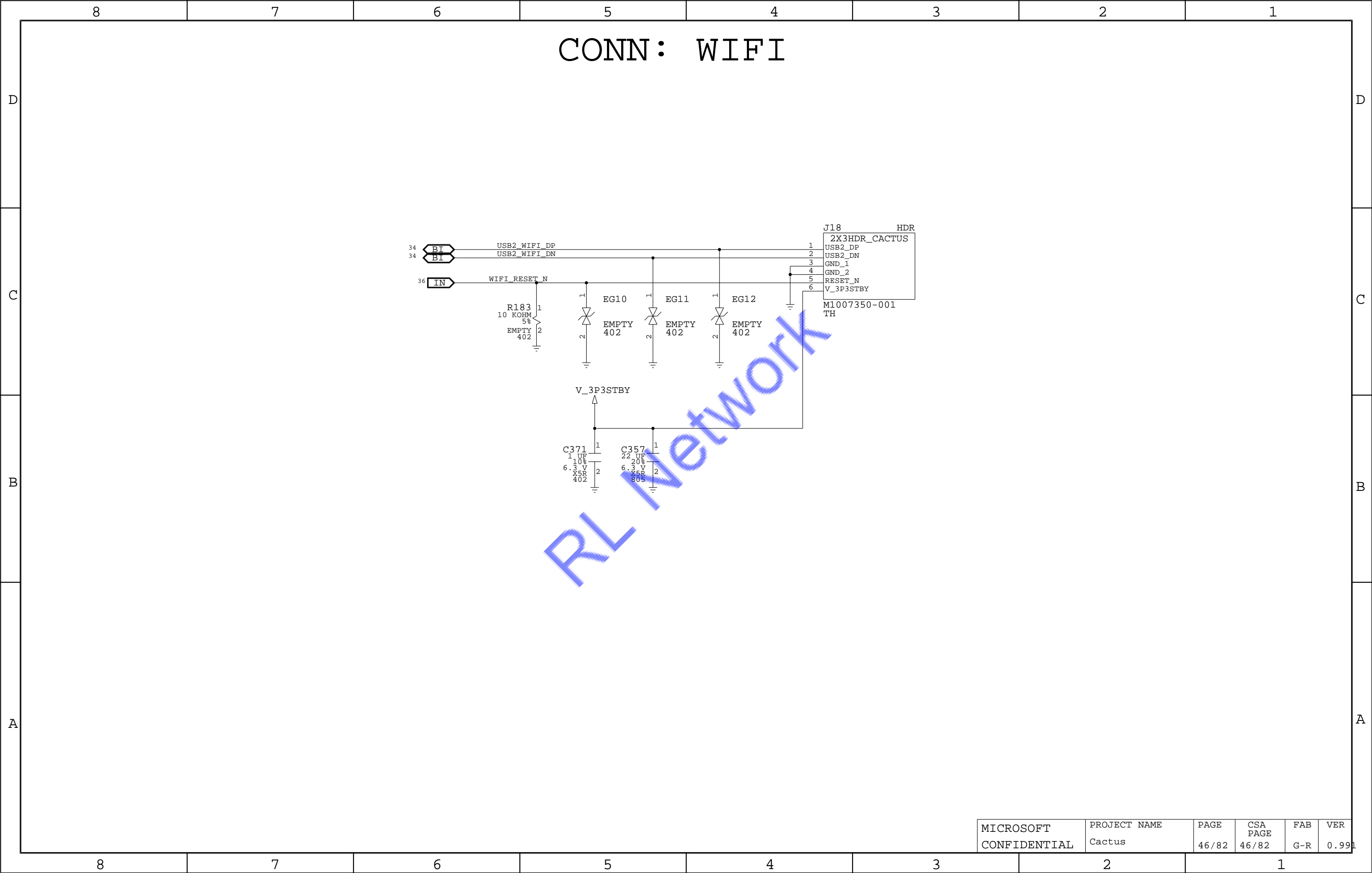


CONN: RJ45 ,TOSLINK



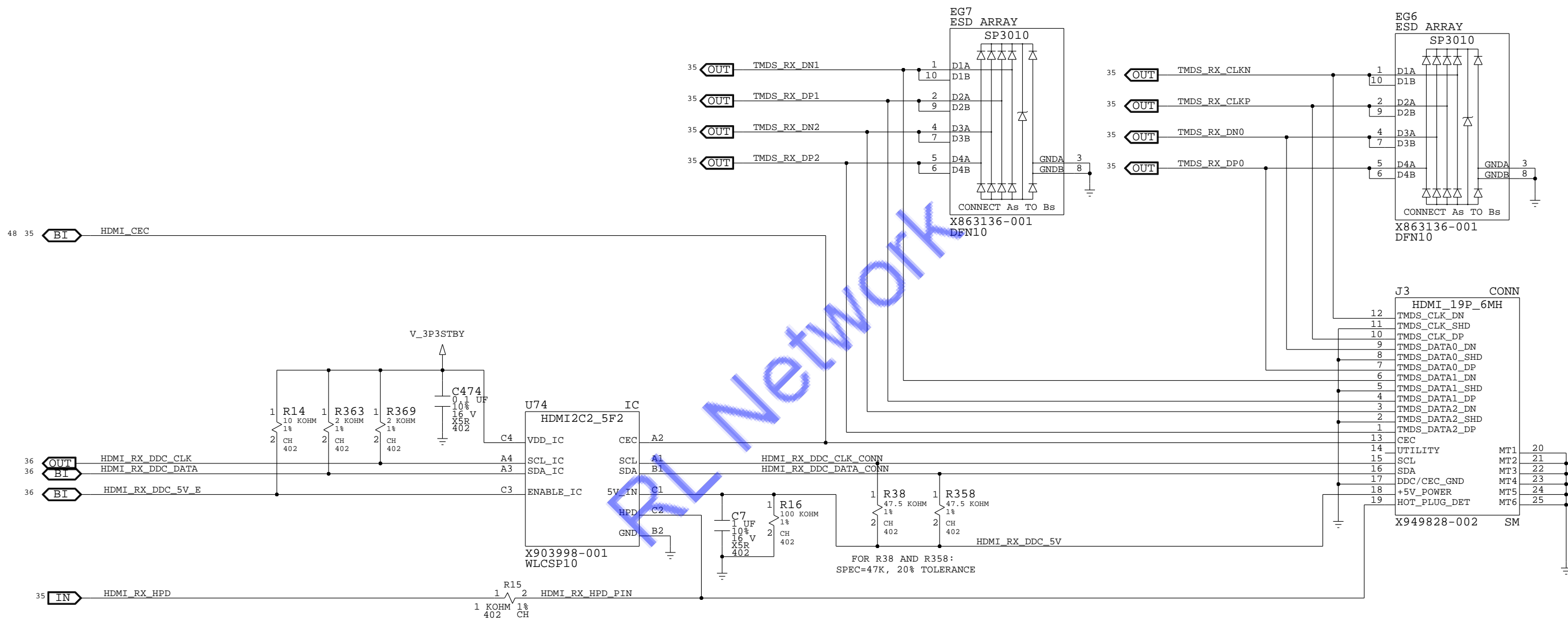
CONN: USB (FRONT & REAR)





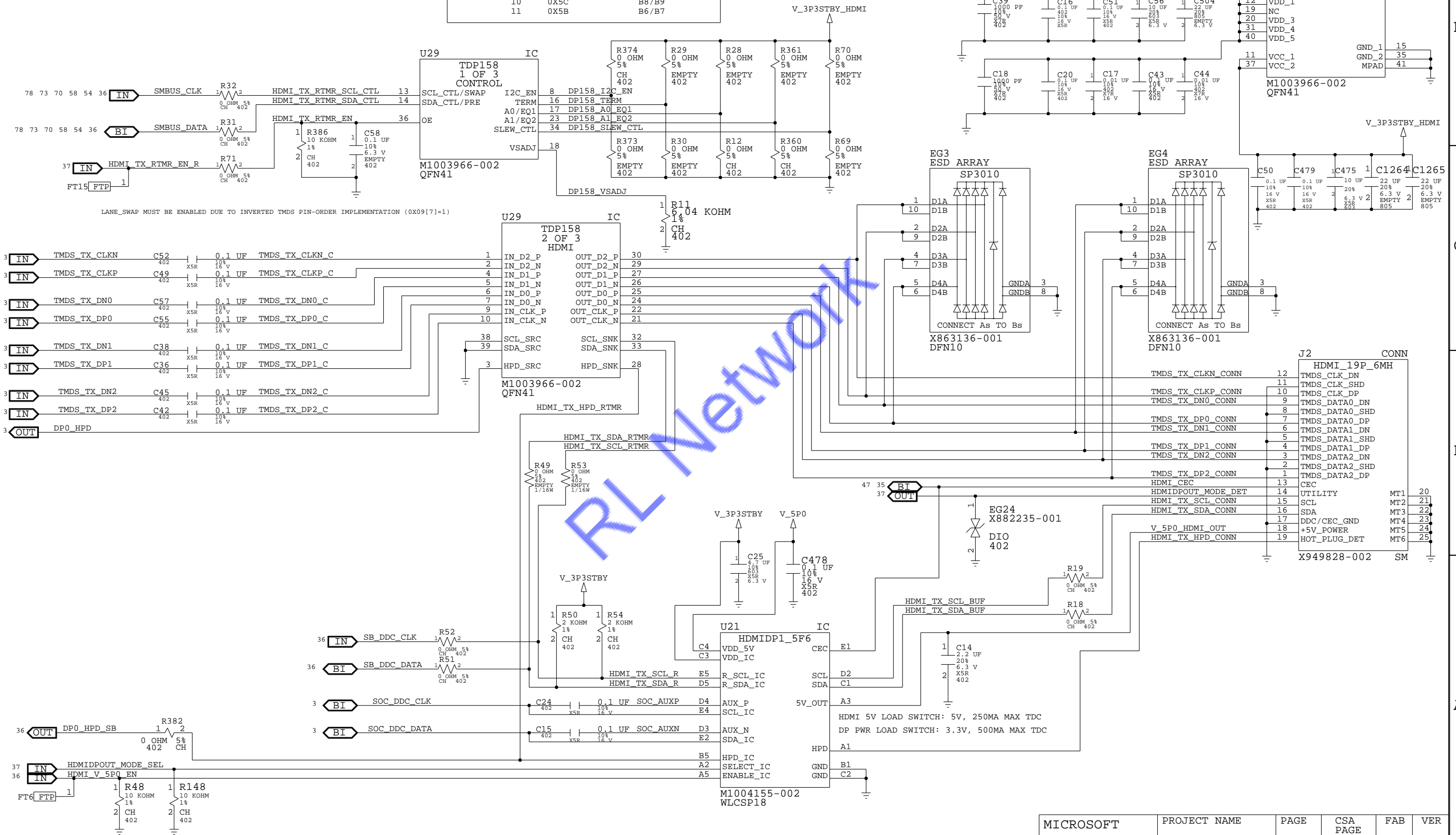


CONN: HDMI IN

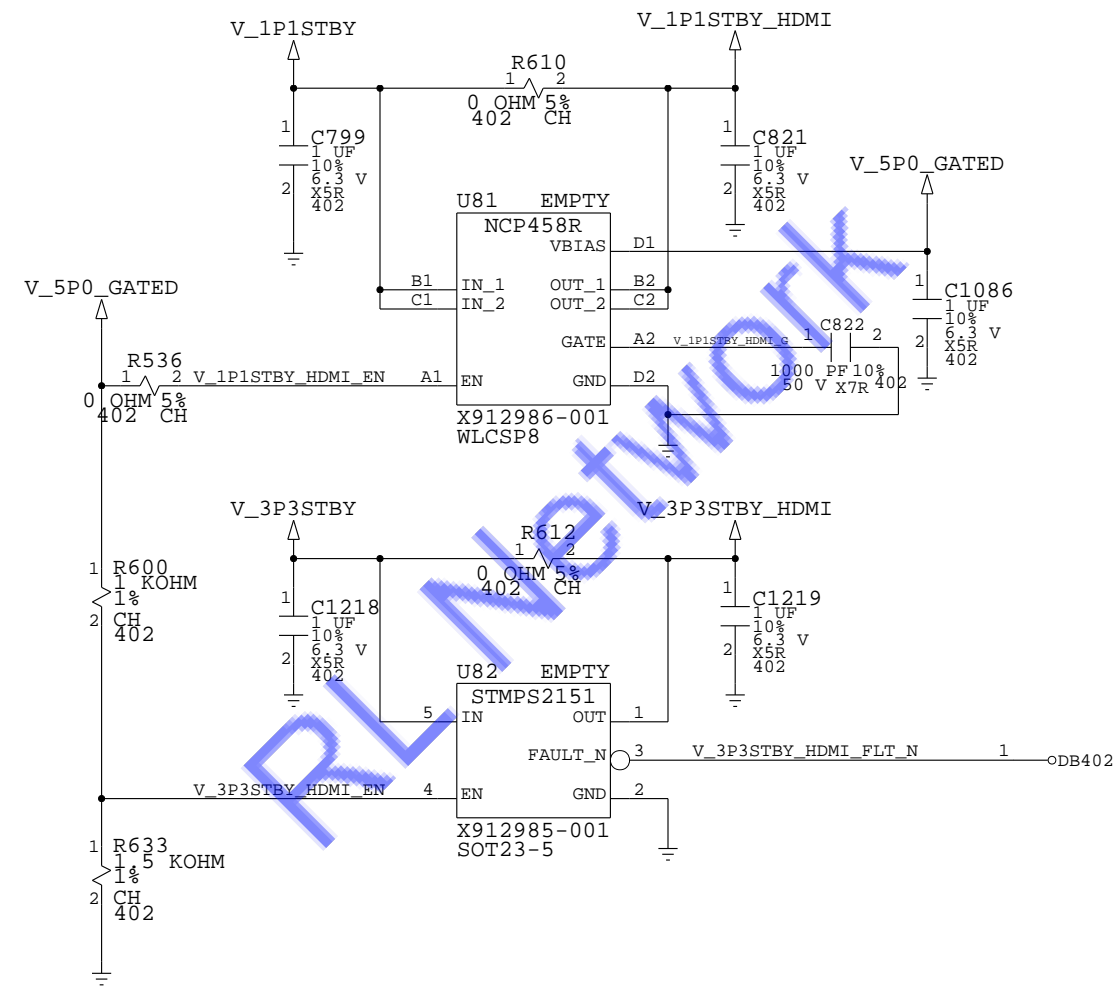


# CONN: HDMI OUT

TDP158 CONTROL SLAVE ADDRESS			
SELECTED	A1/A0	7-BIT ADDRESS	8-BIT ADDRESS
---	00	0X5E	BC/BD
	01	0X5D	BA/BB
	10	0X5C	B8/B9
	11	0X5B	B6/B7



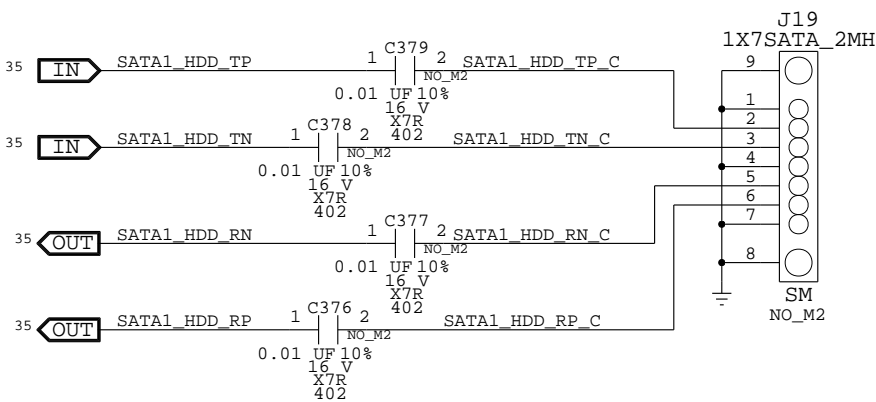
HDMI LOAD SWITCHES



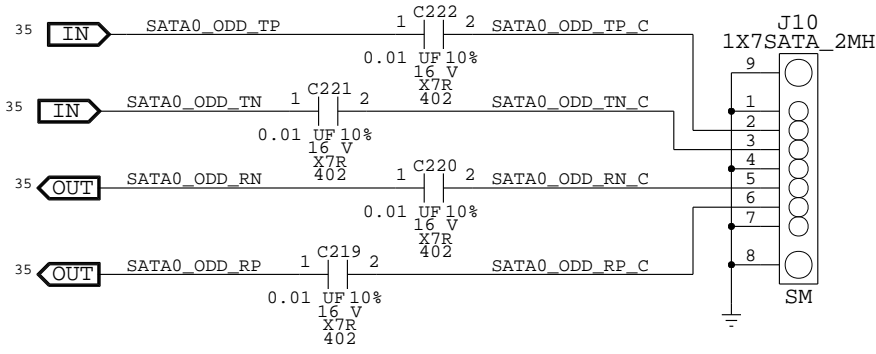
RE-DRIVER	U29	R610	R612	U81	U82
PG1.0	M1003966-001	EMPTY	EMPTY	STUFF	STUFF
PG1.1	M1003966-002	STUFF	STUFF	EMPTY	EMPTY

# CONN: ODD & HDD

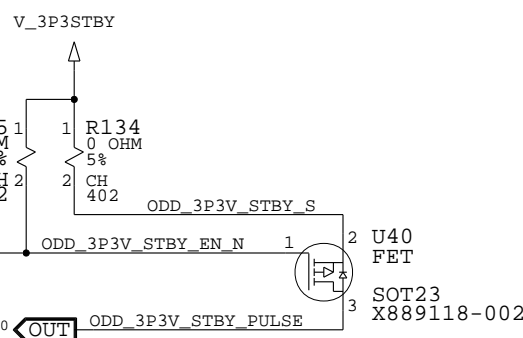
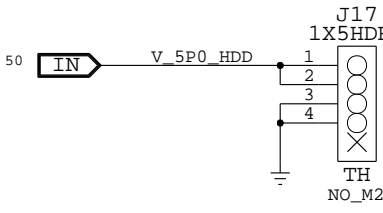
## HDD SATA



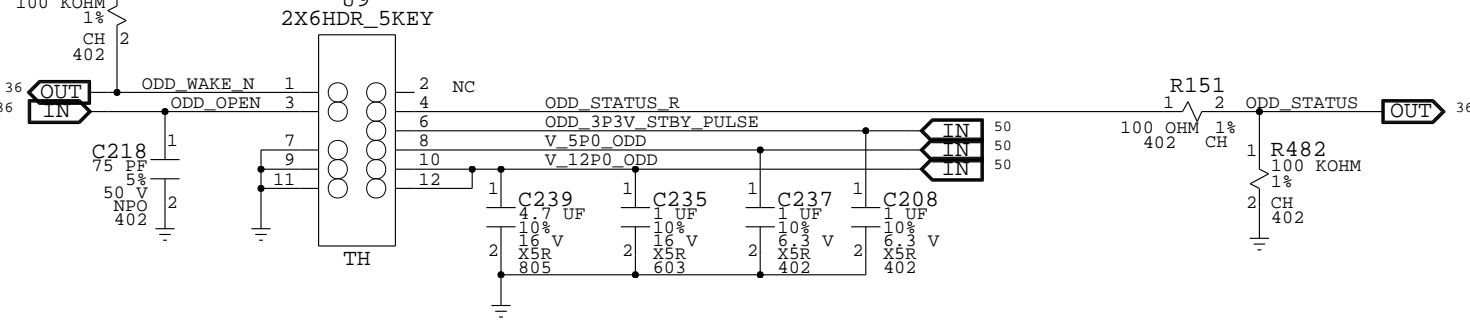
## ODD SATA



## HDD POWER

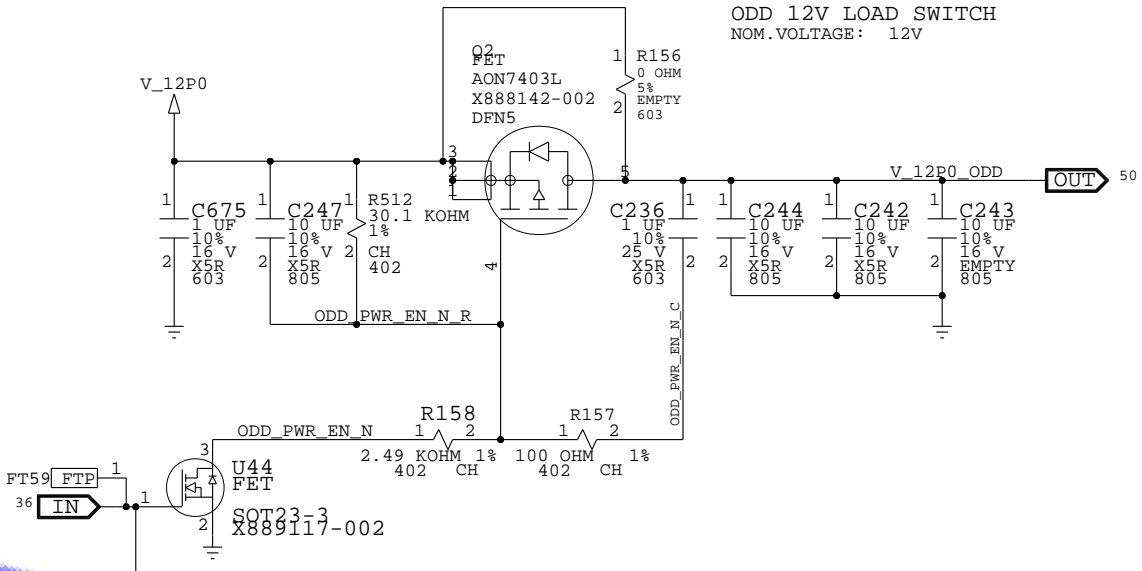


## ODD POWER & GPIOs



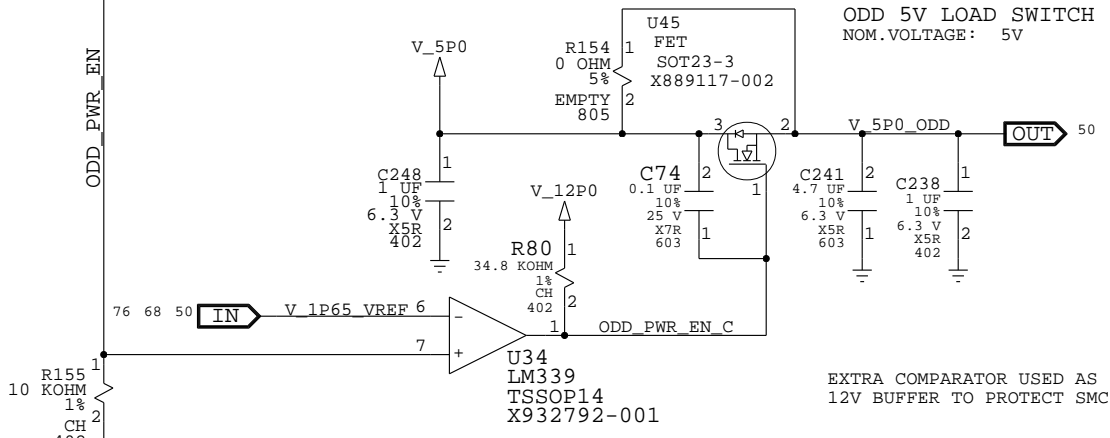
## ODD 12V LOAD SWITCH

NOM.VOLTAGE: 12V



## ODD 5V LOAD SWITCH

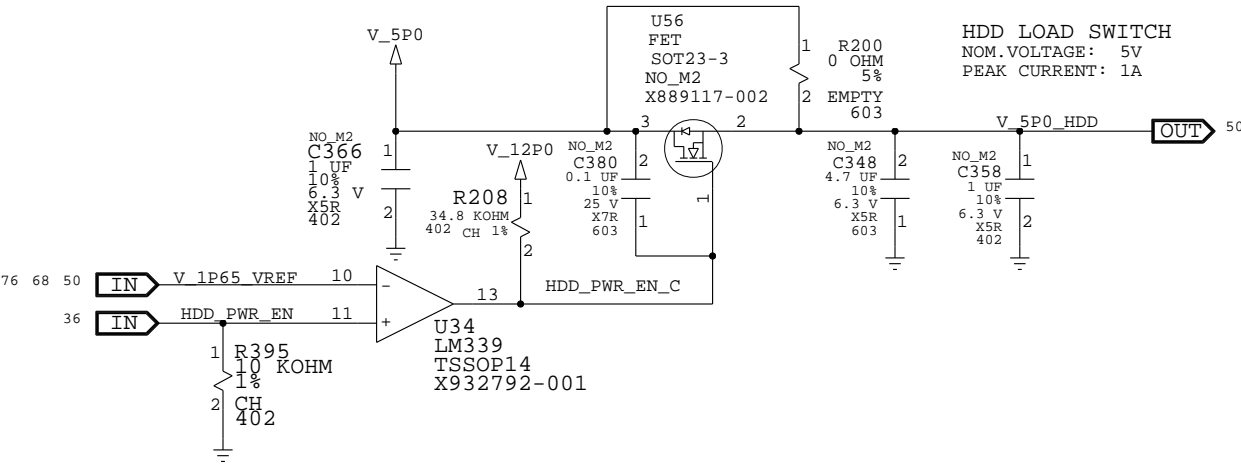
NOM.VOLTAGE: 5V



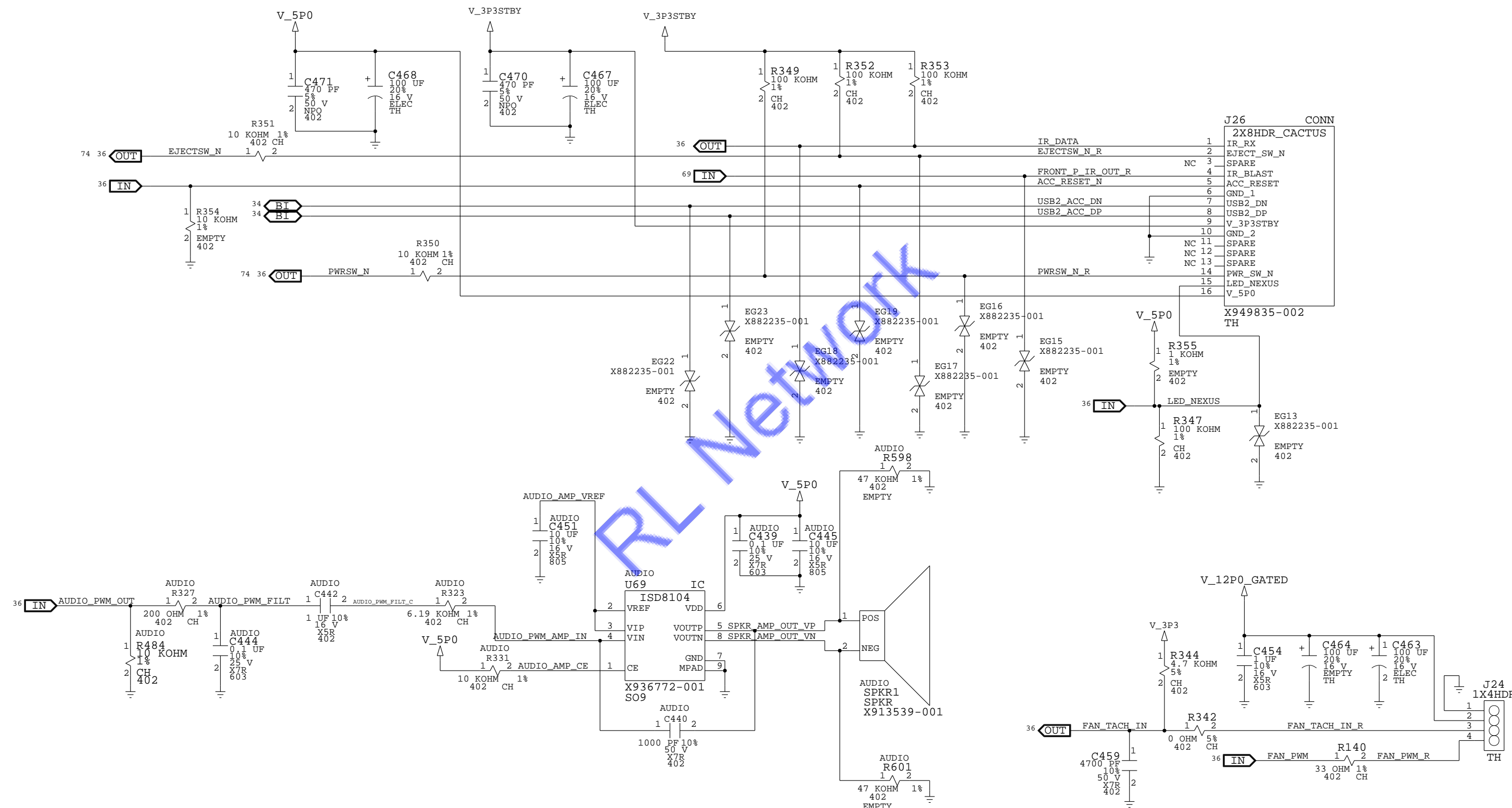
EXTRA COMPARATOR USED AS 12V BUFFER TO PROTECT SMC GPIO

## HDD LOAD SWITCH

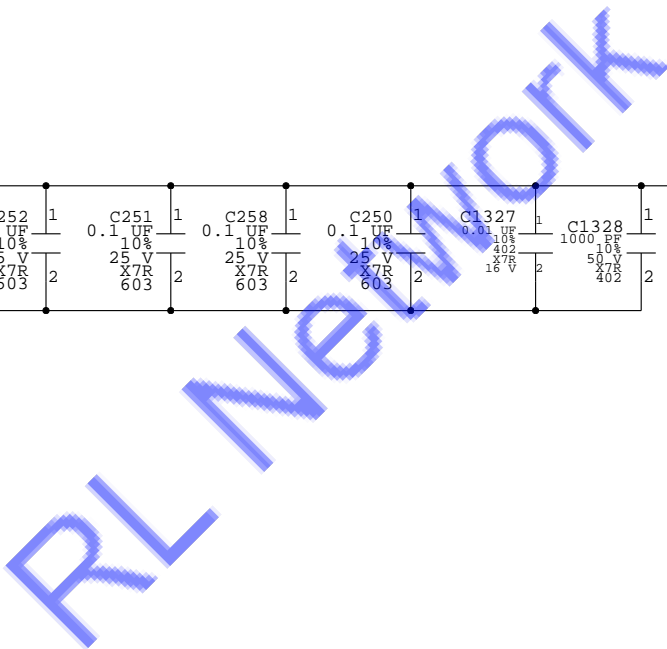
NOM.VOLTAGE: 5V  
PEAK CURRENT: 1A



# CONN: FRONT PANEL, FAN, AUDIO

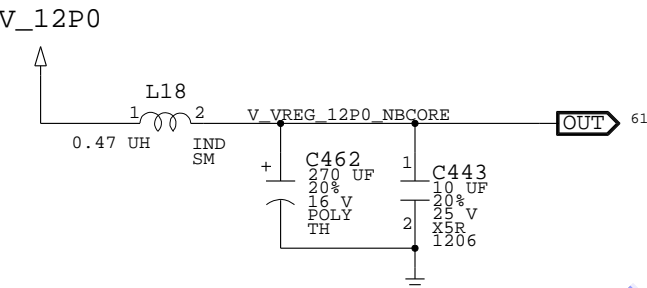




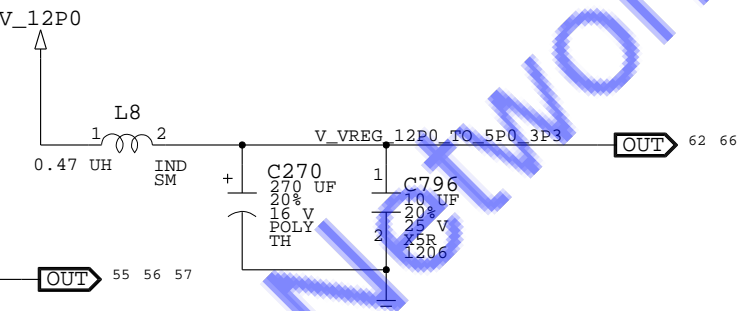


# VREGS: INPUT AND OUTPUT FILTERS

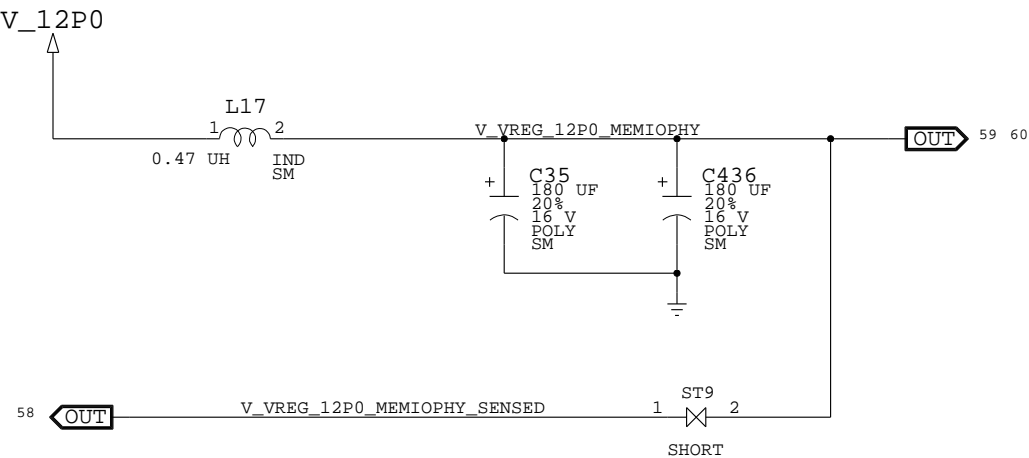
## NBCORE INPUT FILTER



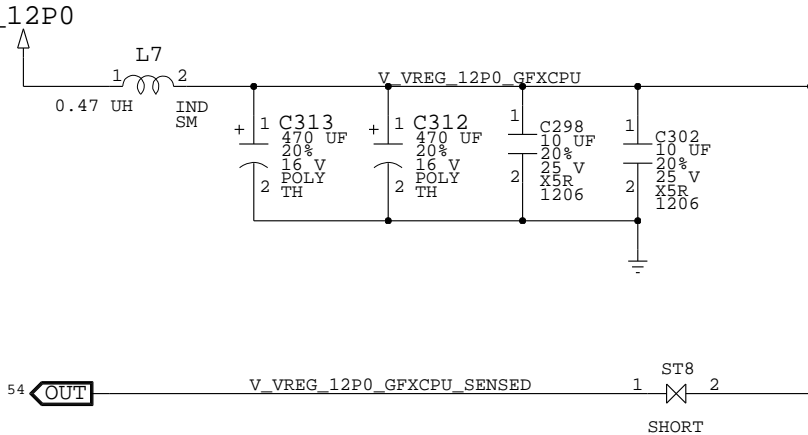
## V\_5P0 AND V\_3P3 INPUT FILTER



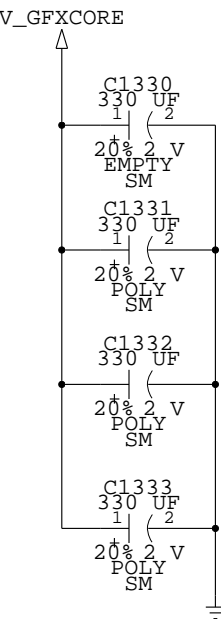
## MEMIO/MEMPHY INPUT FILTER



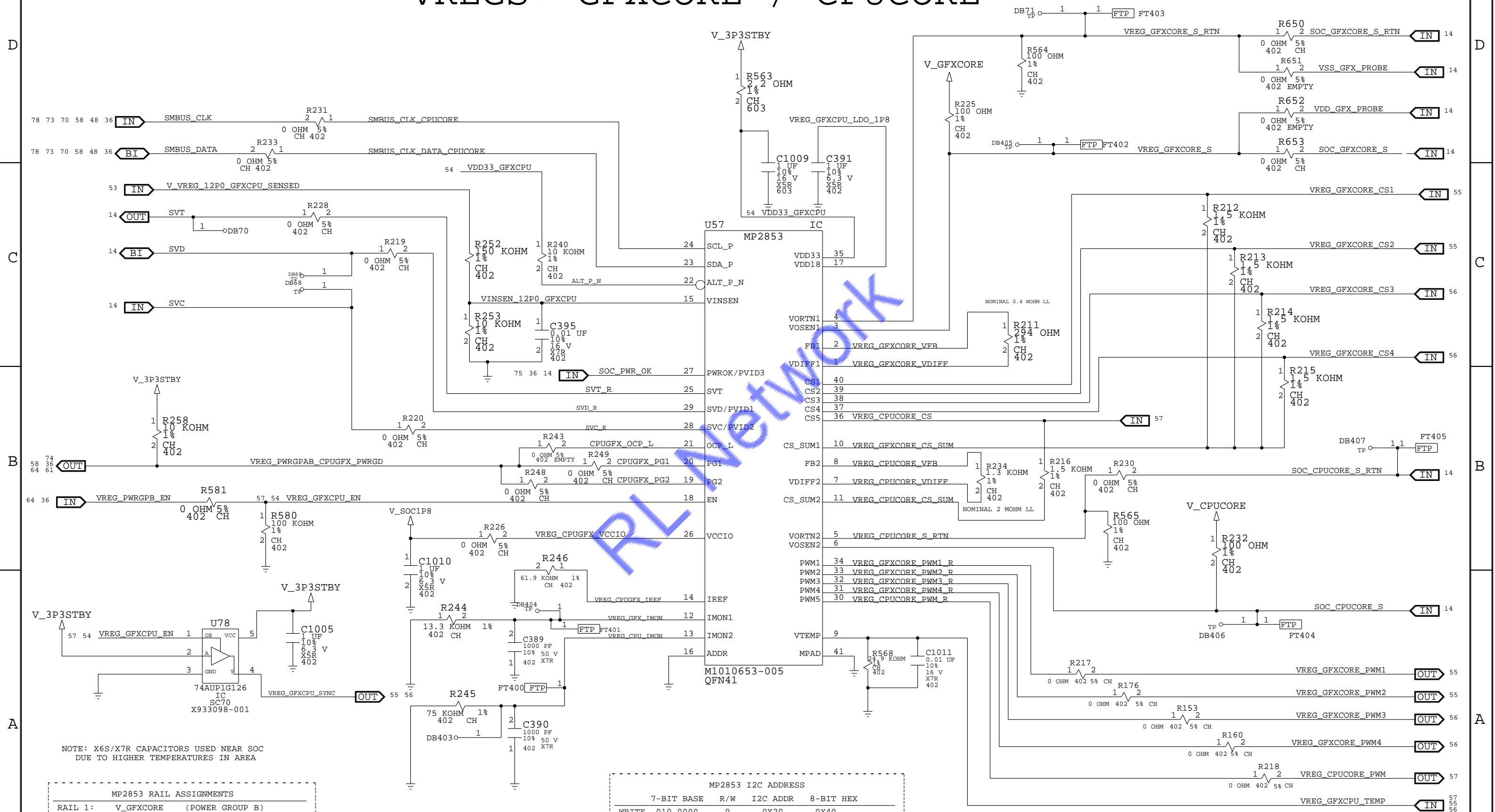
## GFX/CPU INPUT FILTER



## GFXCORE OUTPUT FILTER



```
VREGS:  GFXCORE /  CPUCORE
```

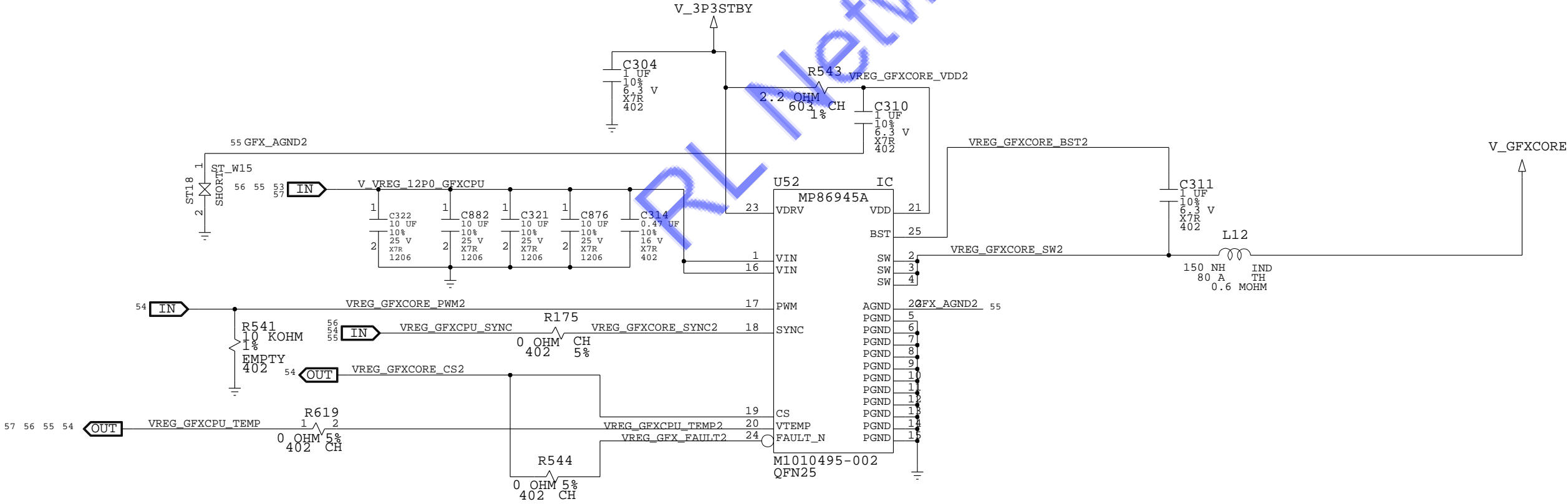
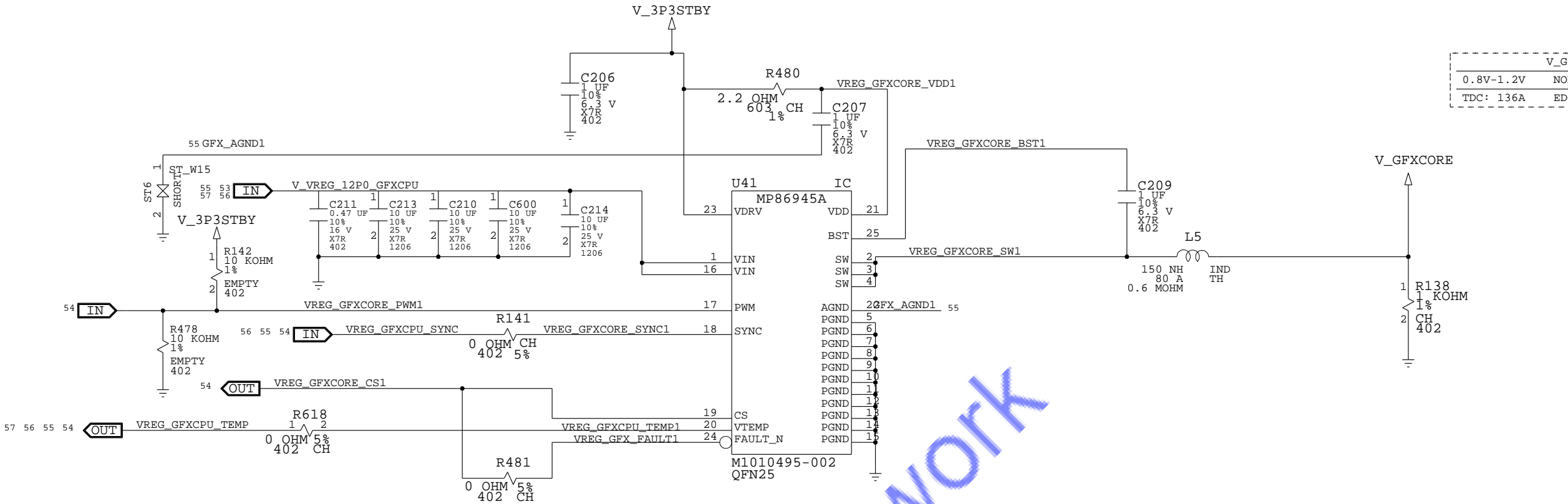


MP2853 I2C ADDRESS						
	7-BIT BASE			R/W	I2C ADDR	8-BIT HEX
WRITE	010	0000		0	0X20	0X40
READ	010	0000		1	0X20	0X41

MP2853 RAIL ASSIGNMENTS		
RAIL 1:	V_GFXCORE	(POWER GROUP B)
RAIL 2:	V_CPUCORE	(POWER GROUP B)

VREGS: GFXCORE OUTPUT PHASE 1 & 2

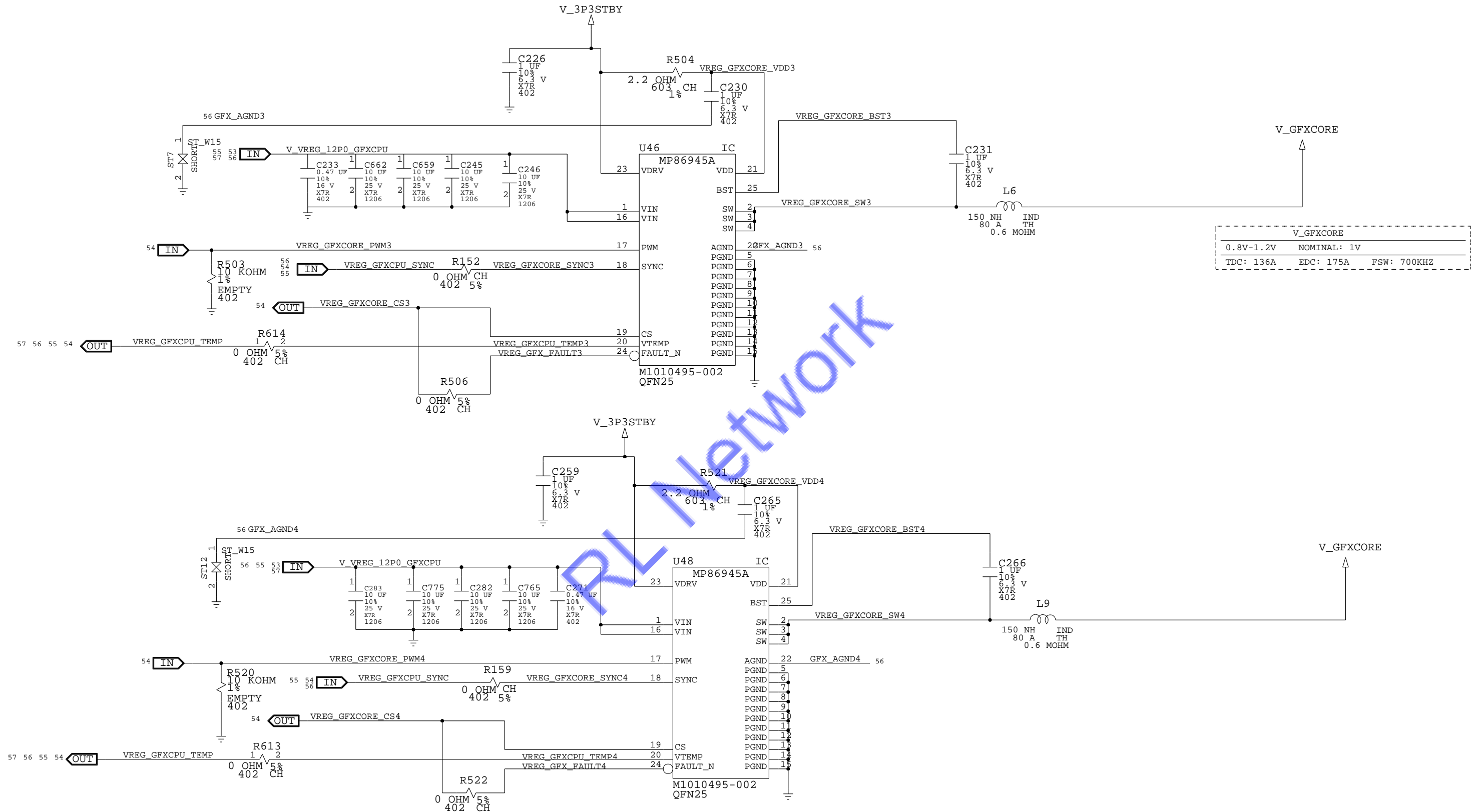
V_GFXCORE		
0.8V-1.2V	NOMINAL: 1V	
TDC: 136A	EDC: 175A	FSW: 700KHZ



NOTE: X6S/X7R CAPACITORS USED NEAR SOC  
DUE TO HIGHER TEMPERATURES IN AREA

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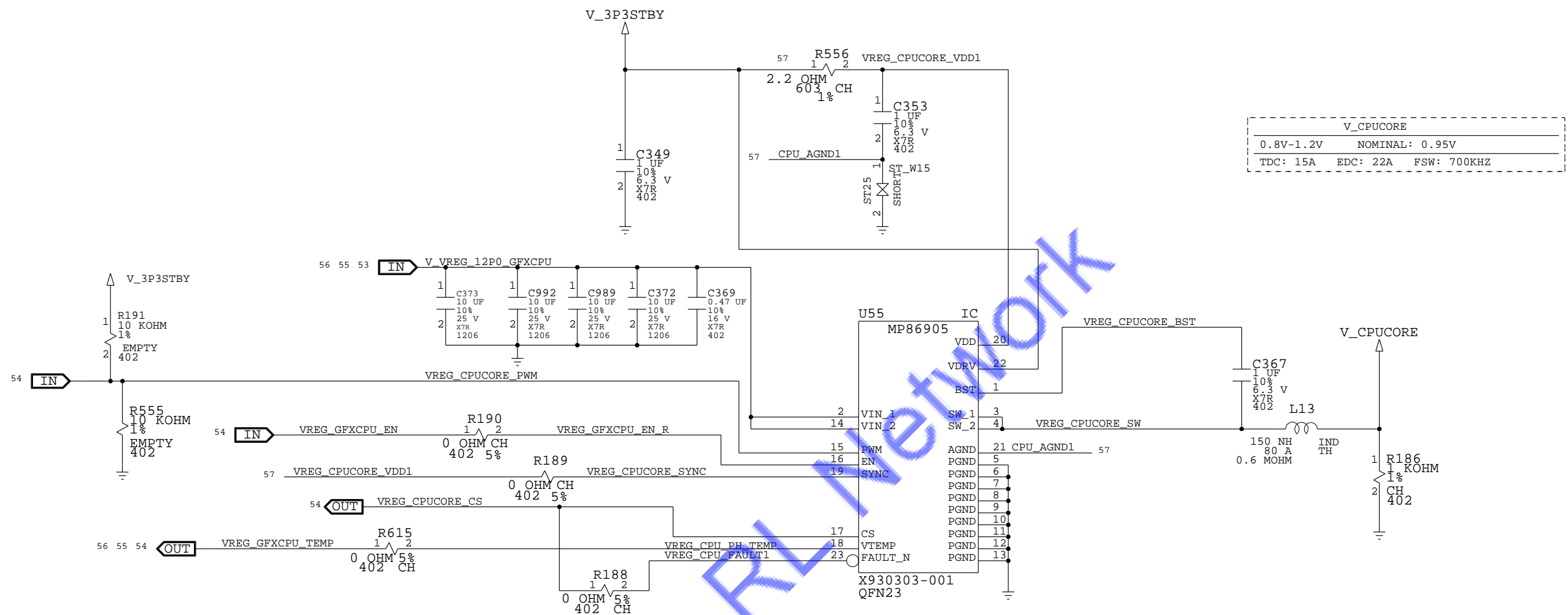
```
VREGS:  GFXCORE  OUTPUT  PHASE  3  &  4
```



NOTE: X6S/X7R CAPACITORS USED NEAR SOC  
DUE TO HIGHER TEMPERATURES IN AREA

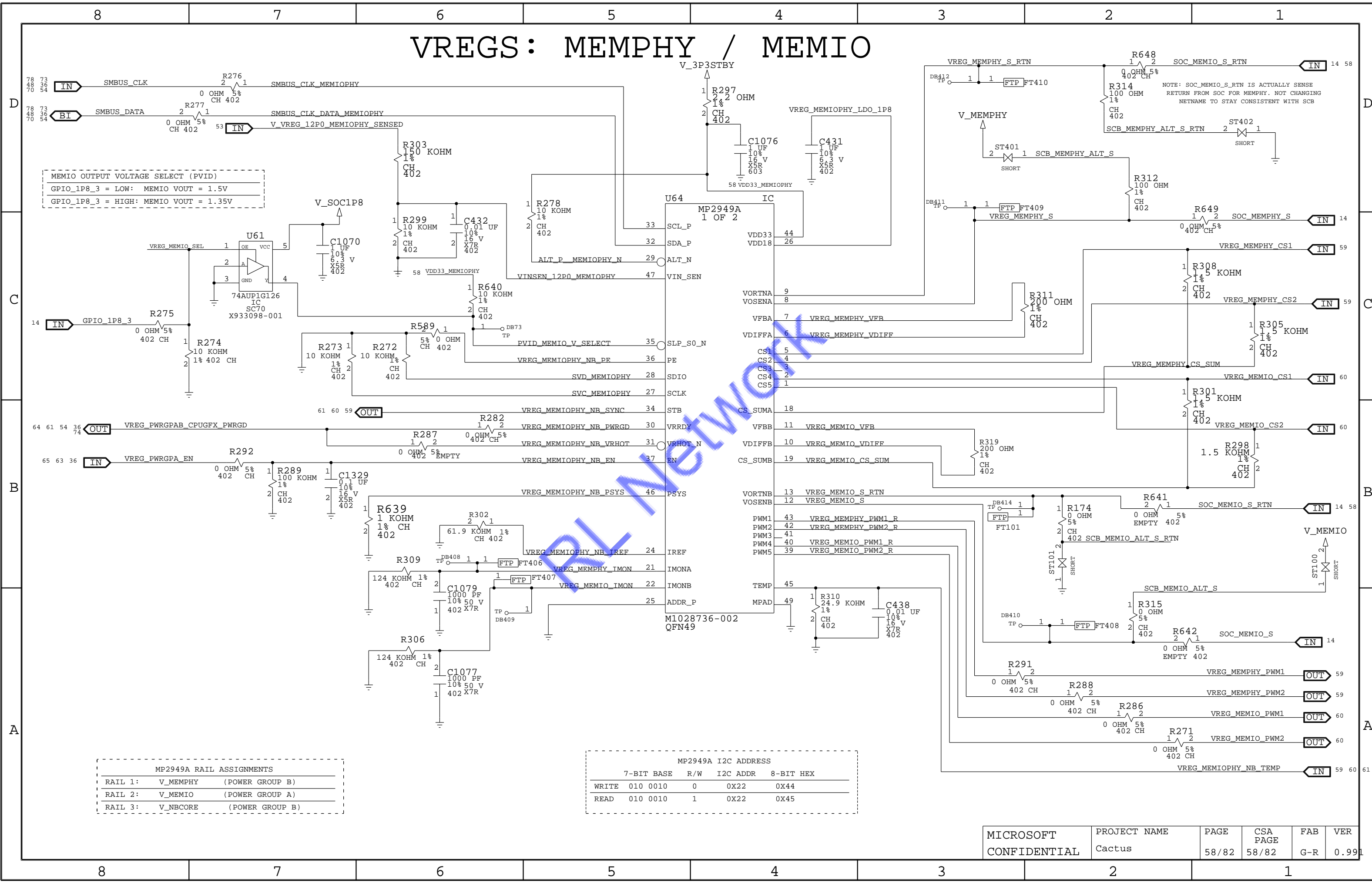


# VREGS: CPUCORE OUTPUT PHASE

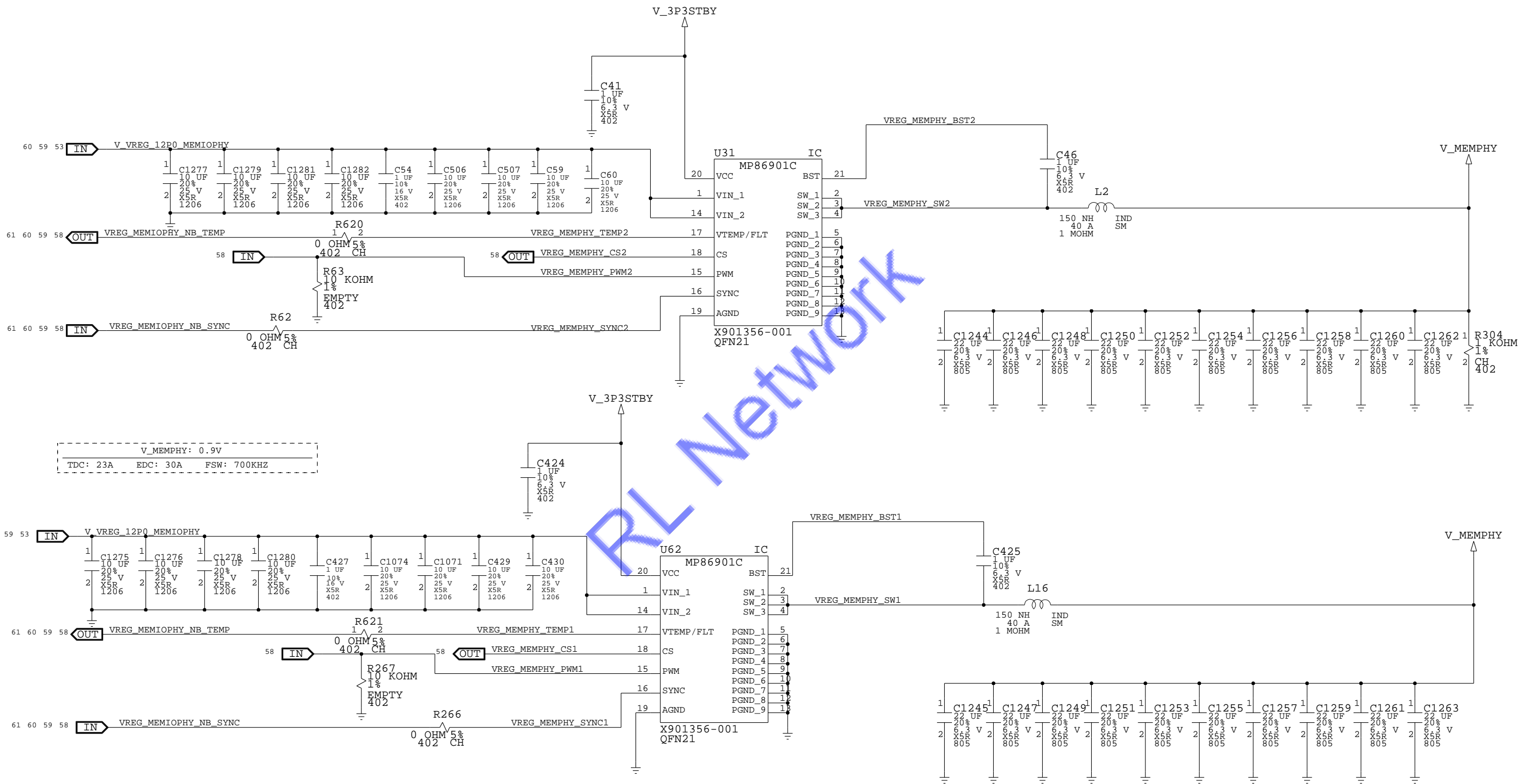


NOTE: X6S/X7R CAPACITORS USED NEAR SOC  
DUE TO HIGHER TEMPERATURES IN AREA

# VREGS: MEMPHY / MEMIO



VREGS: MEMPHY OUTPUT



VREGS: MEMIO OUTPUT

V_MEMIO					
1.35-1.5V NOMINAL: 1.5V					
TDC(RETAIL): 20A		EDC(RETAIL): 23A		FSW: 700KHZ	
TDC(XDK): 25A		EDC(XDK): 30A		FSW: 700KHZ	

D

C

B

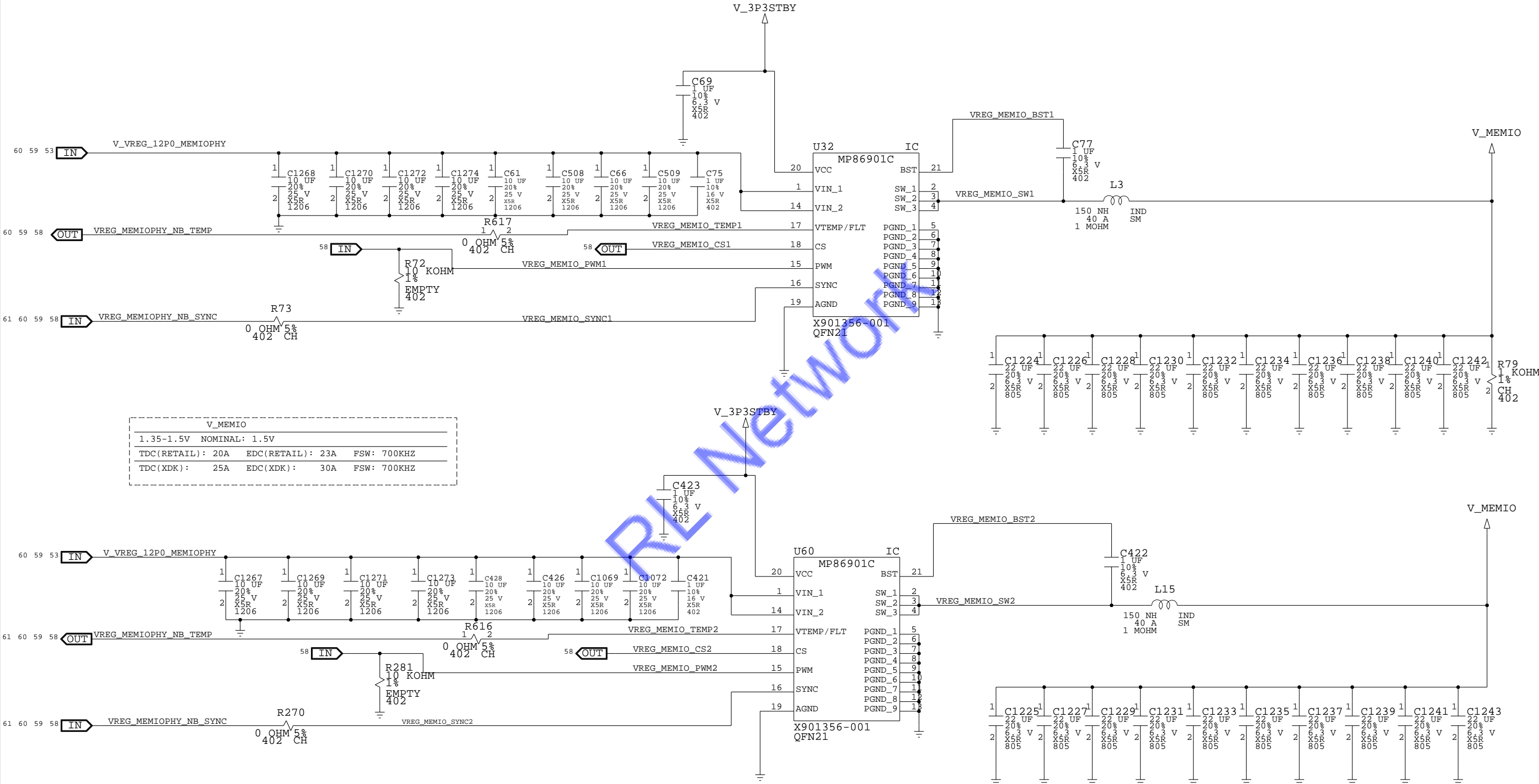
A

D

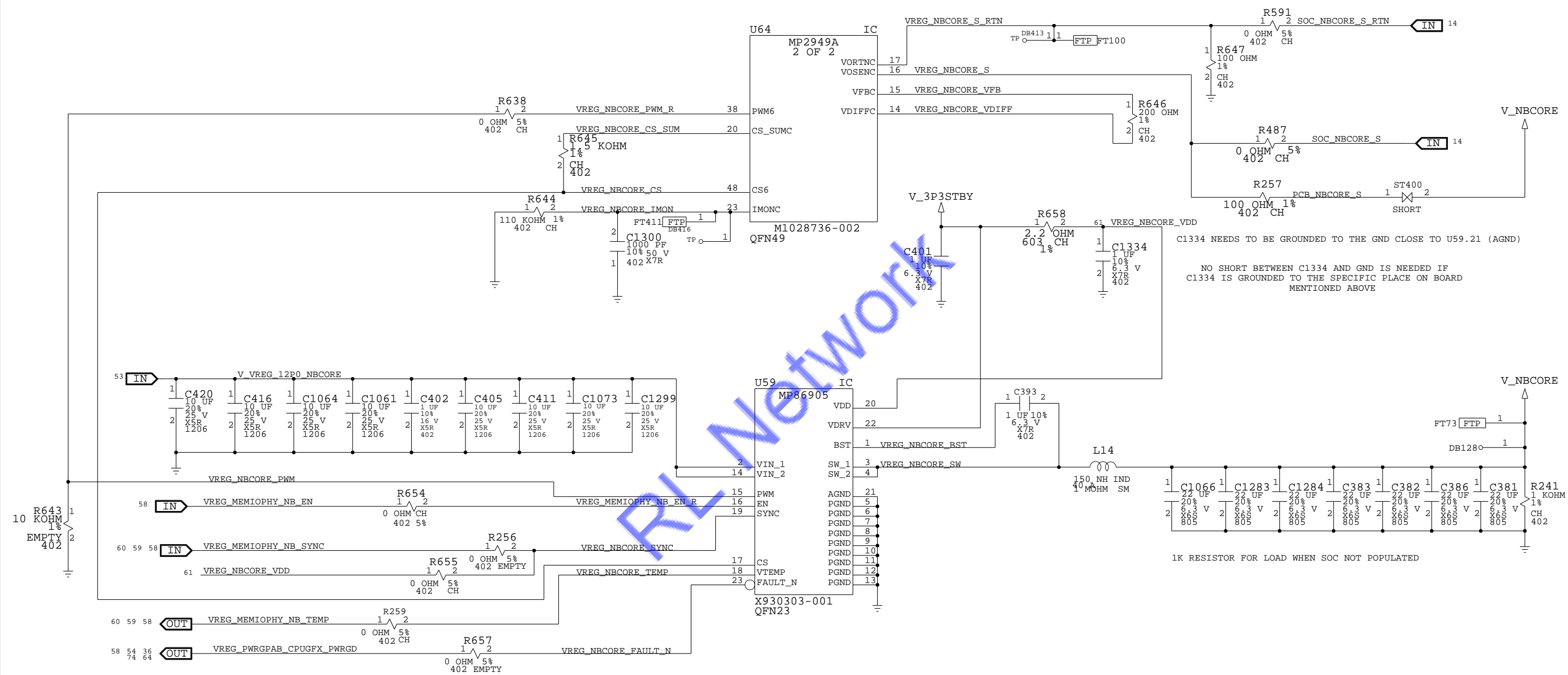
C

B

A



VREGS : NBCORE

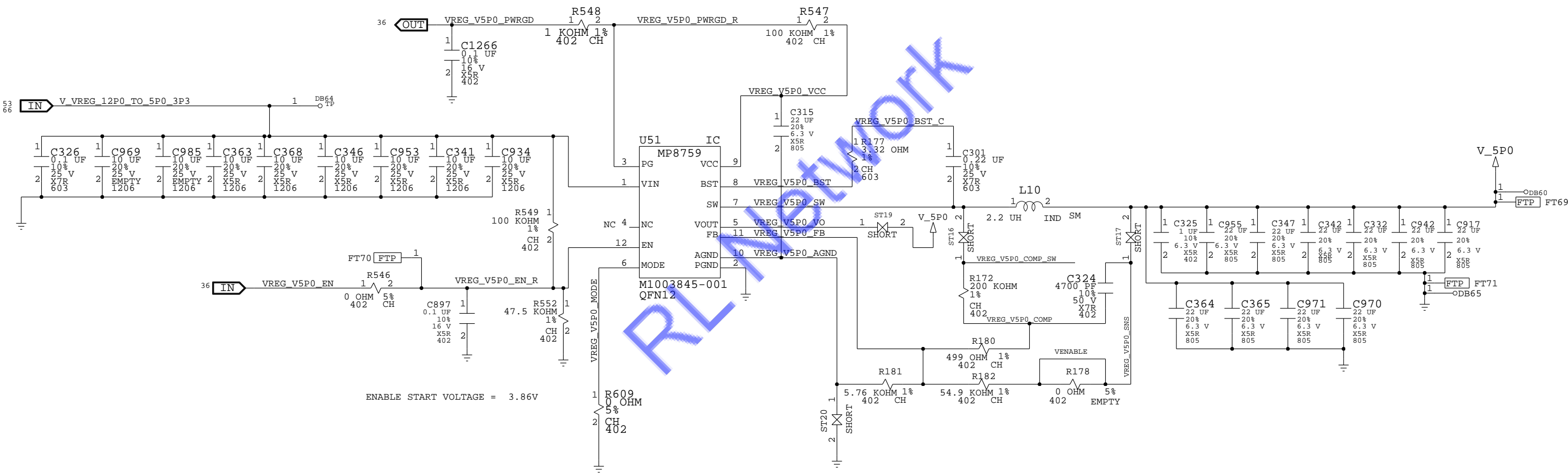


V_NBCORE			
0.8V-1.2V	NOMINAL: 0.95V		
TDC: 16A	EDC: 25A	FSW: 700KHZ	

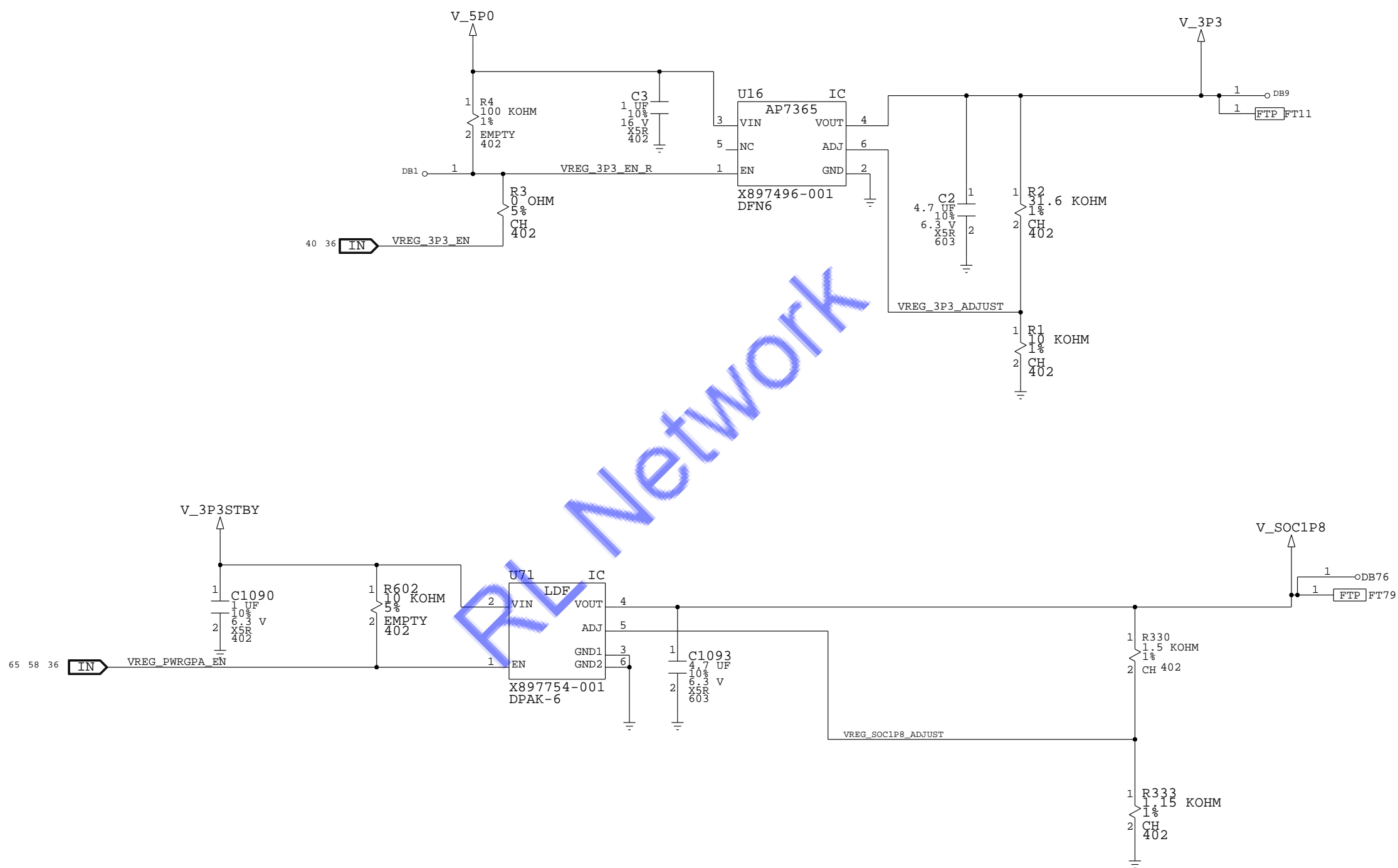


# VREGS: V5P0

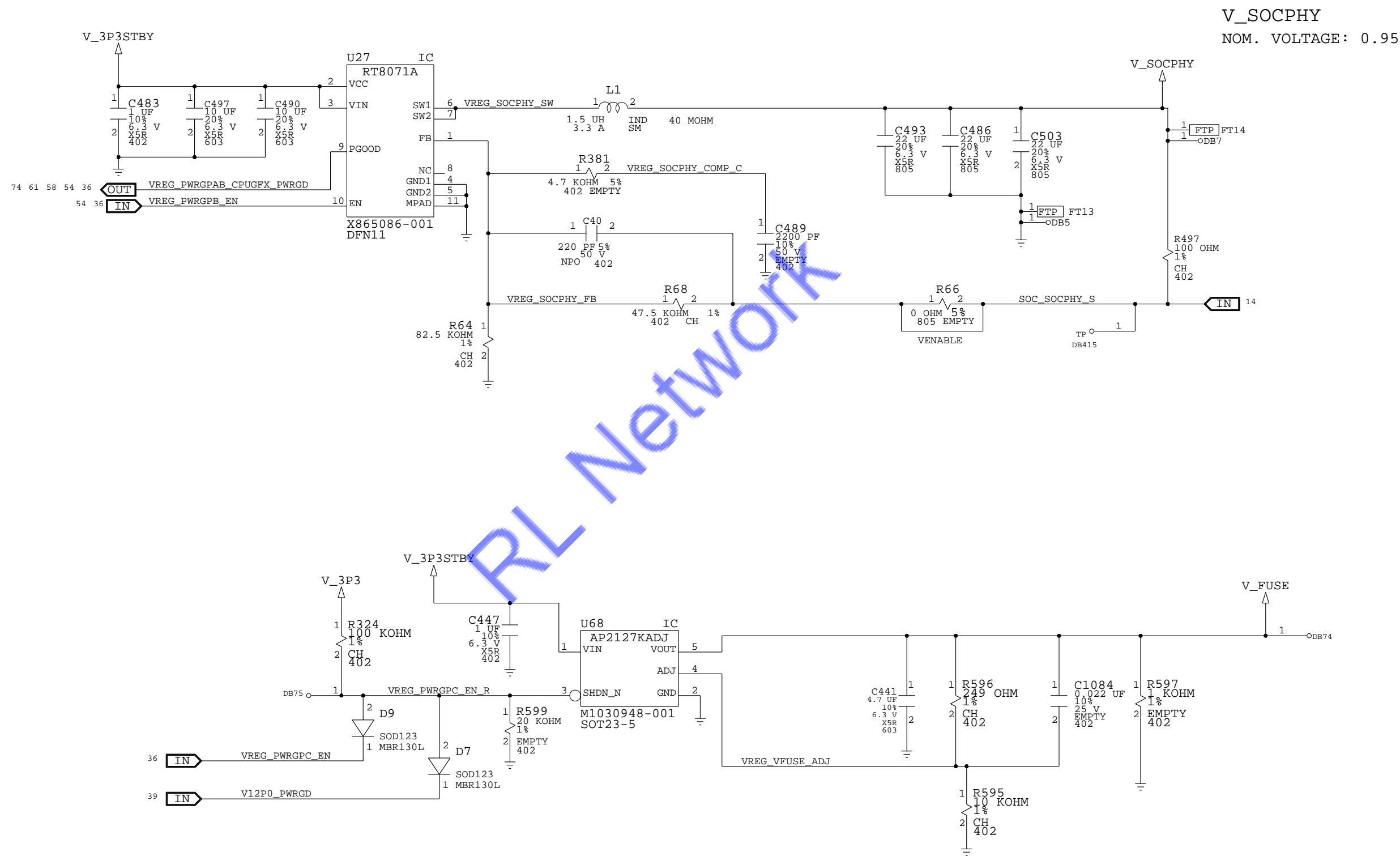
V\_5P0  
NOM. VOLTAGE: 5.1



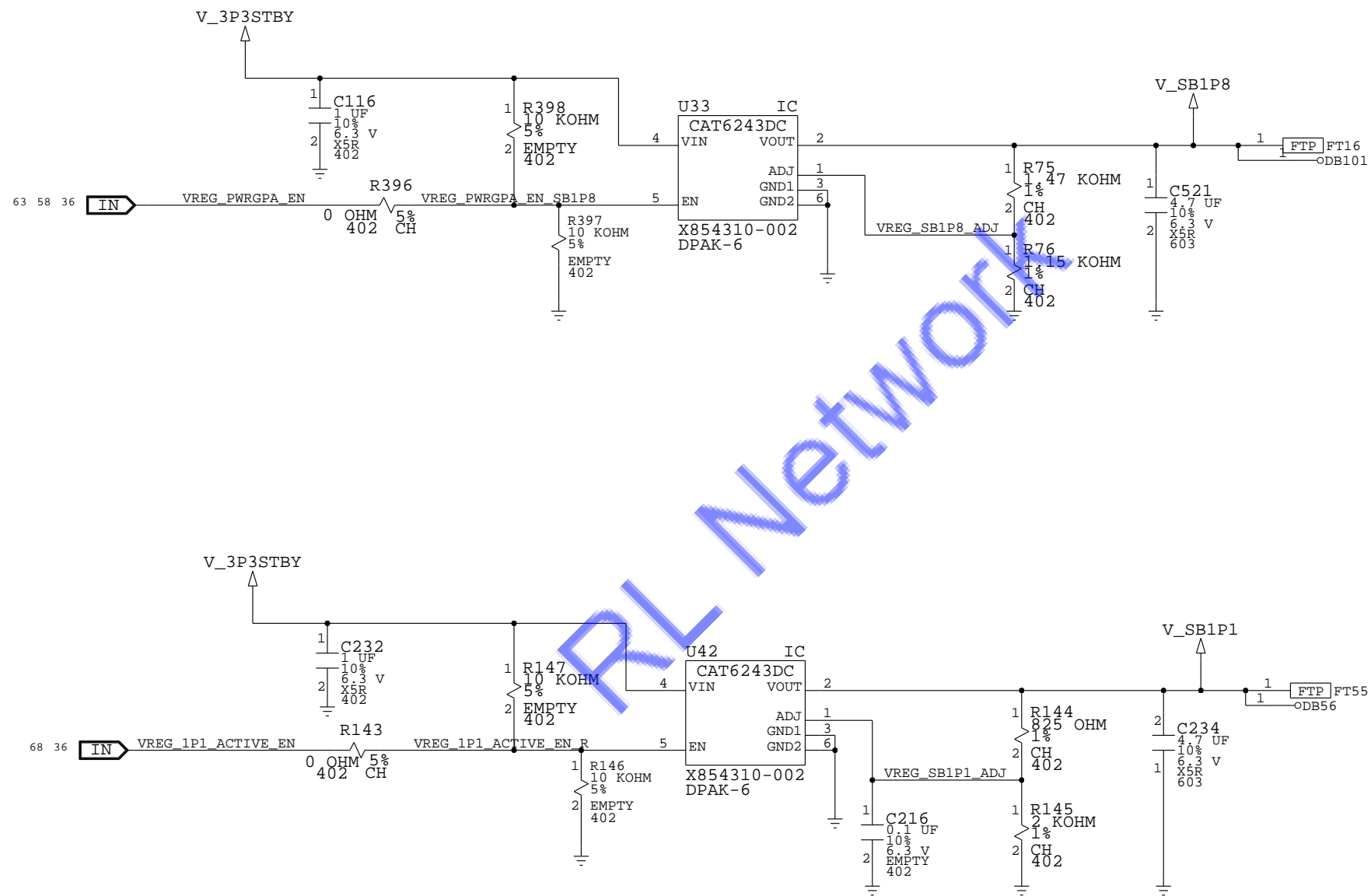
VREGS: V3P3, VSOC1P8



VREGS: VSOCPHY/VFUSE

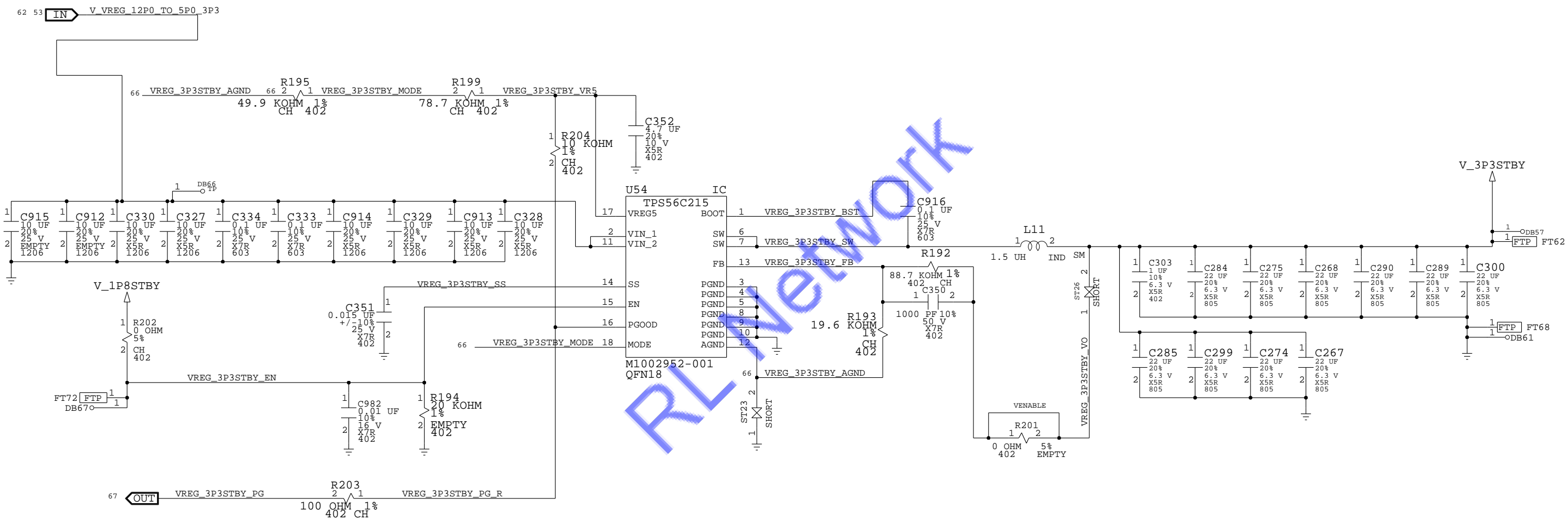


VREGS: V\_SB1P8, V\_SB1P1



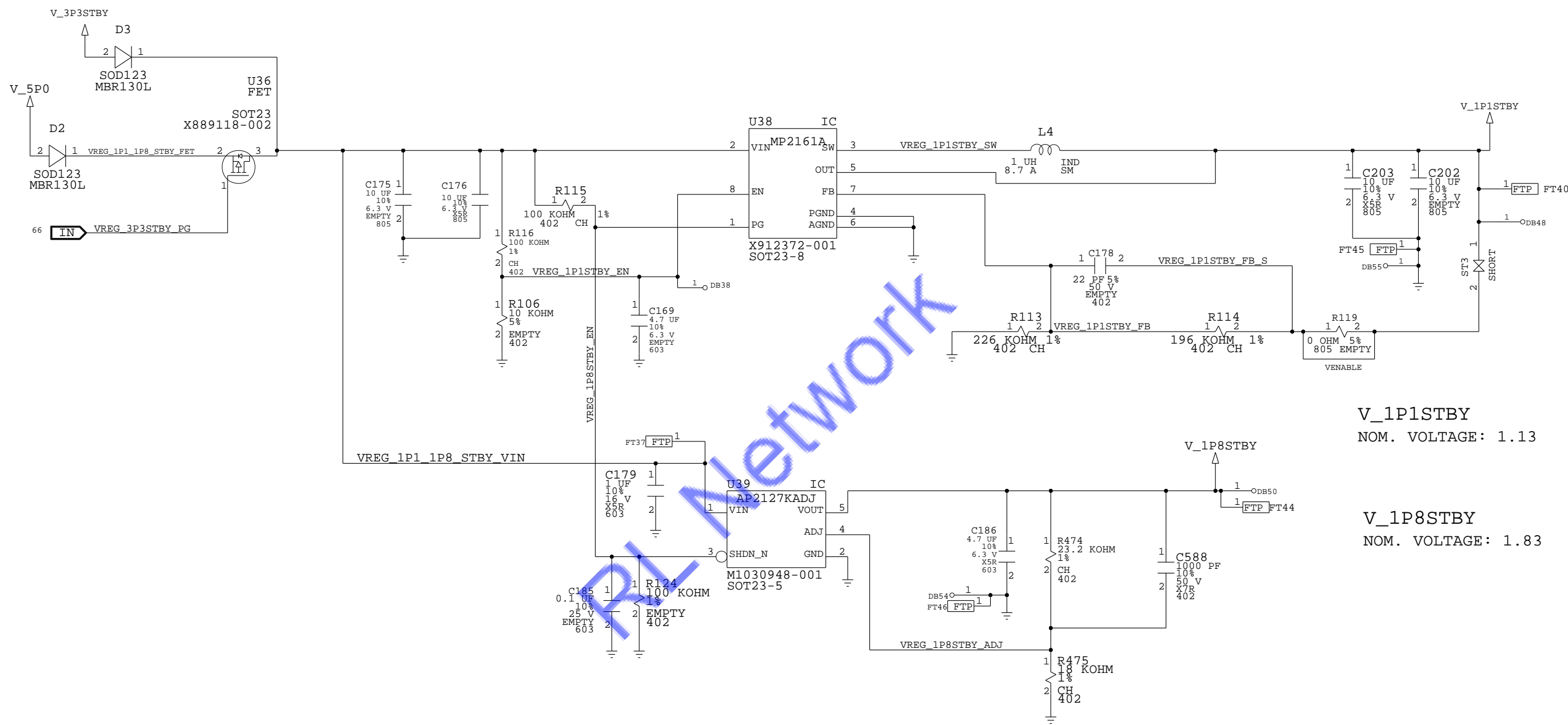
VREGS: V3P3 STANDBY

V\_3P3STBY  
NOM. VOLTAGE: 3.32





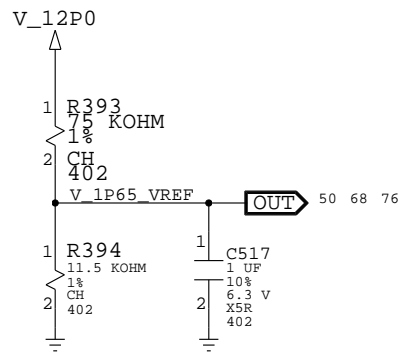
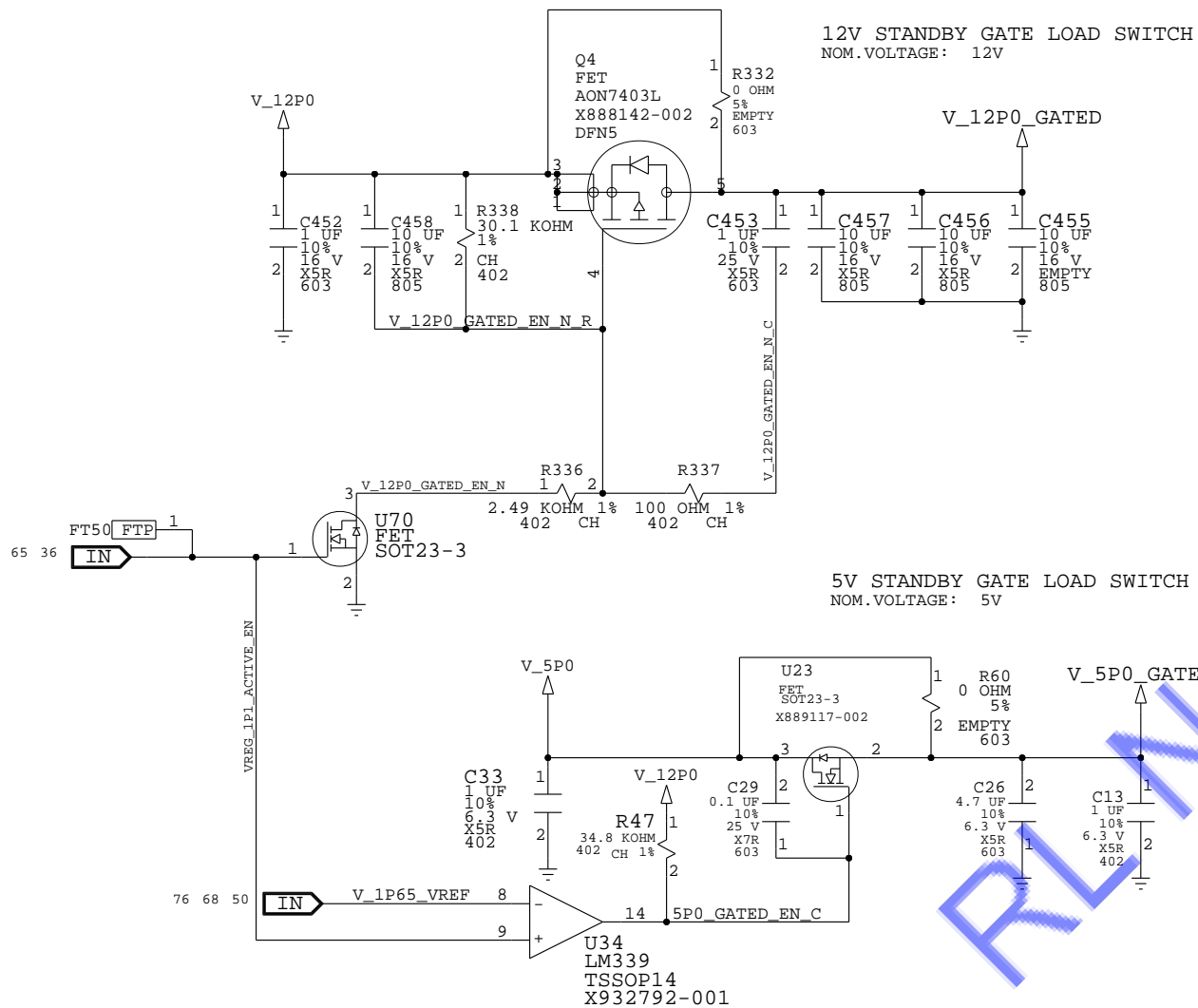
# VREGS: V1P1 STANDBY, V1P8 STANDBY



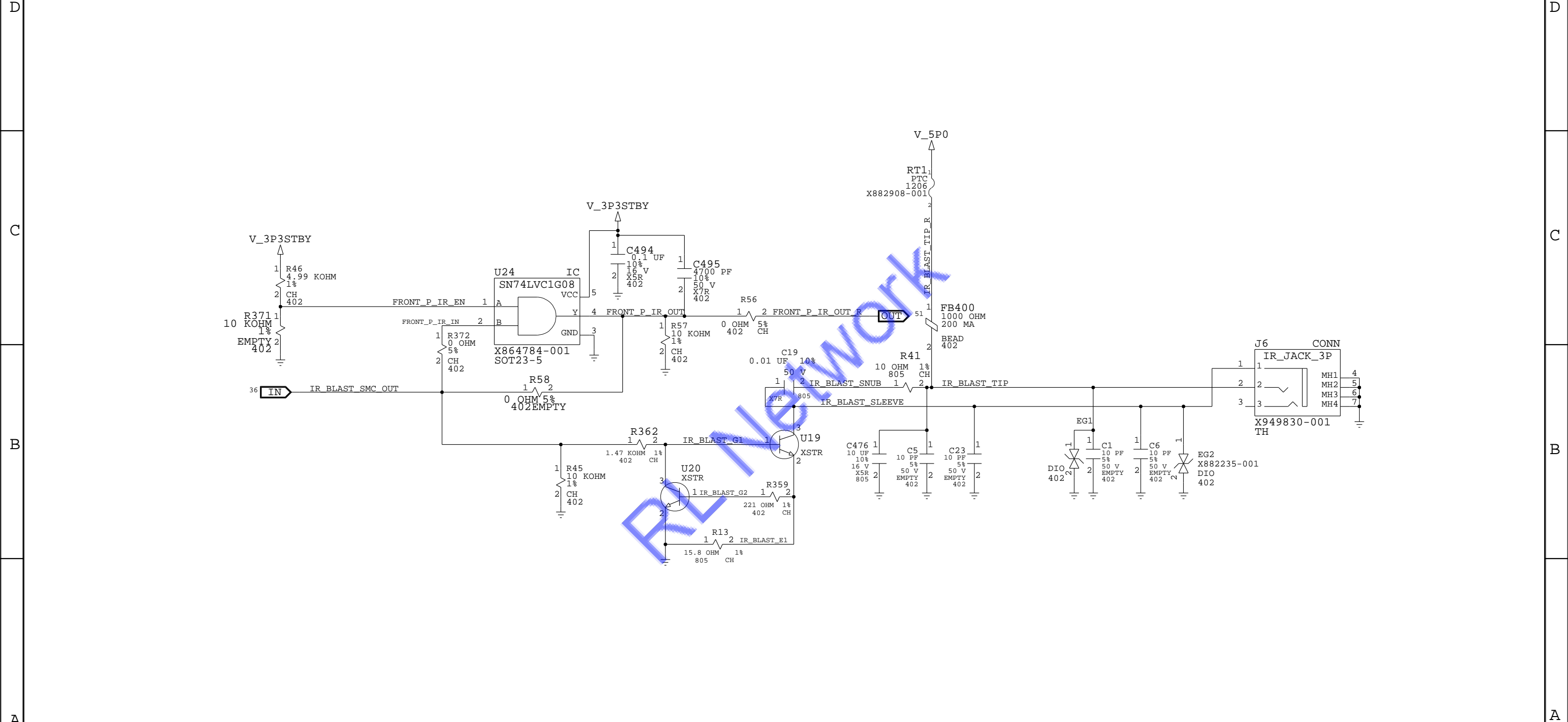
V\_1P1STBY  
NOM. VOLTAGE: 1.13

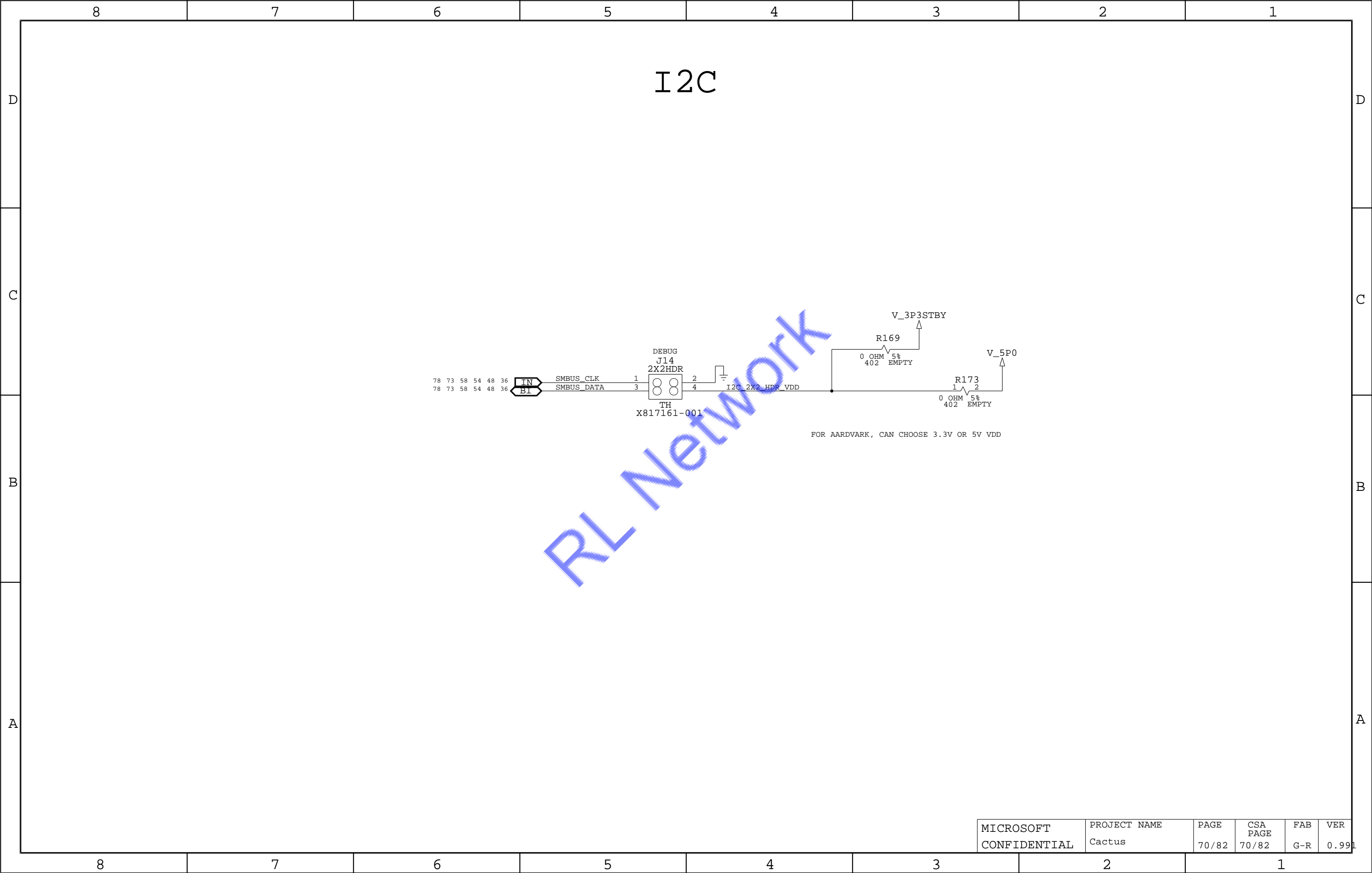
V\_1P8STBY  
NOM. VOLTAGE: 1.83

# STANDBY GATES



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---





MARGIN: SOCPHY, SOC1P8

# BLANK

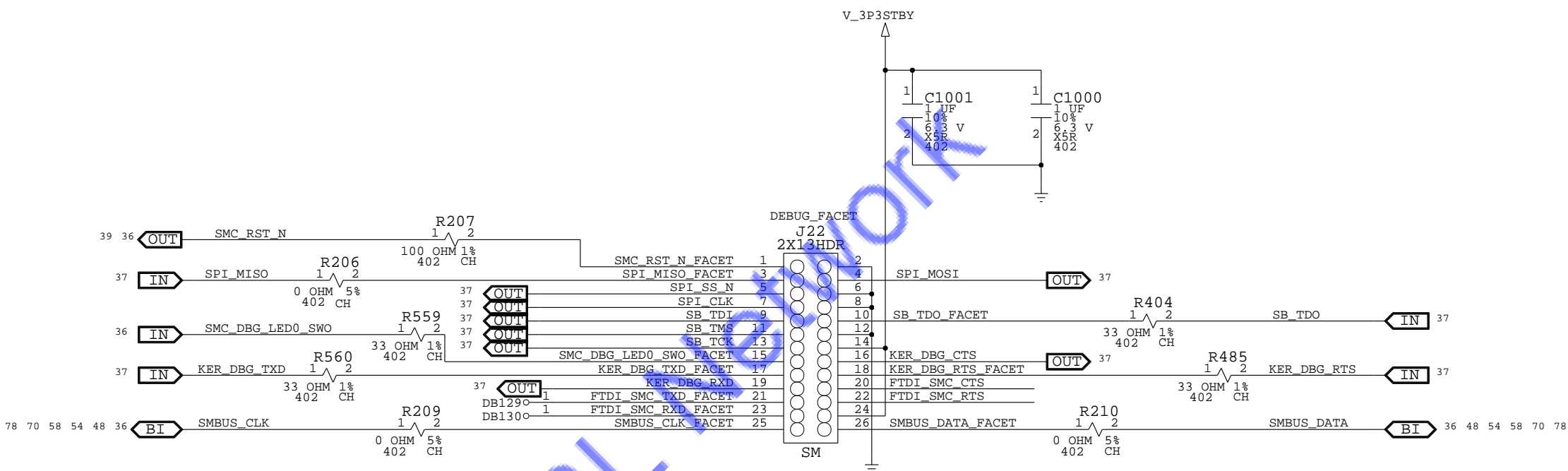
BLANK

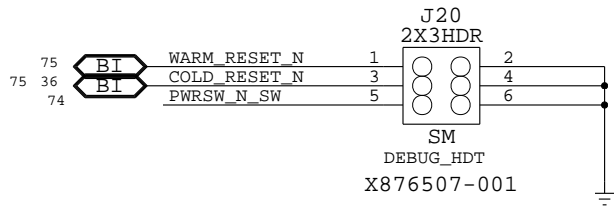
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
CONFIDENTIAL	Cactus	71/82	71/82	G-R	0.99



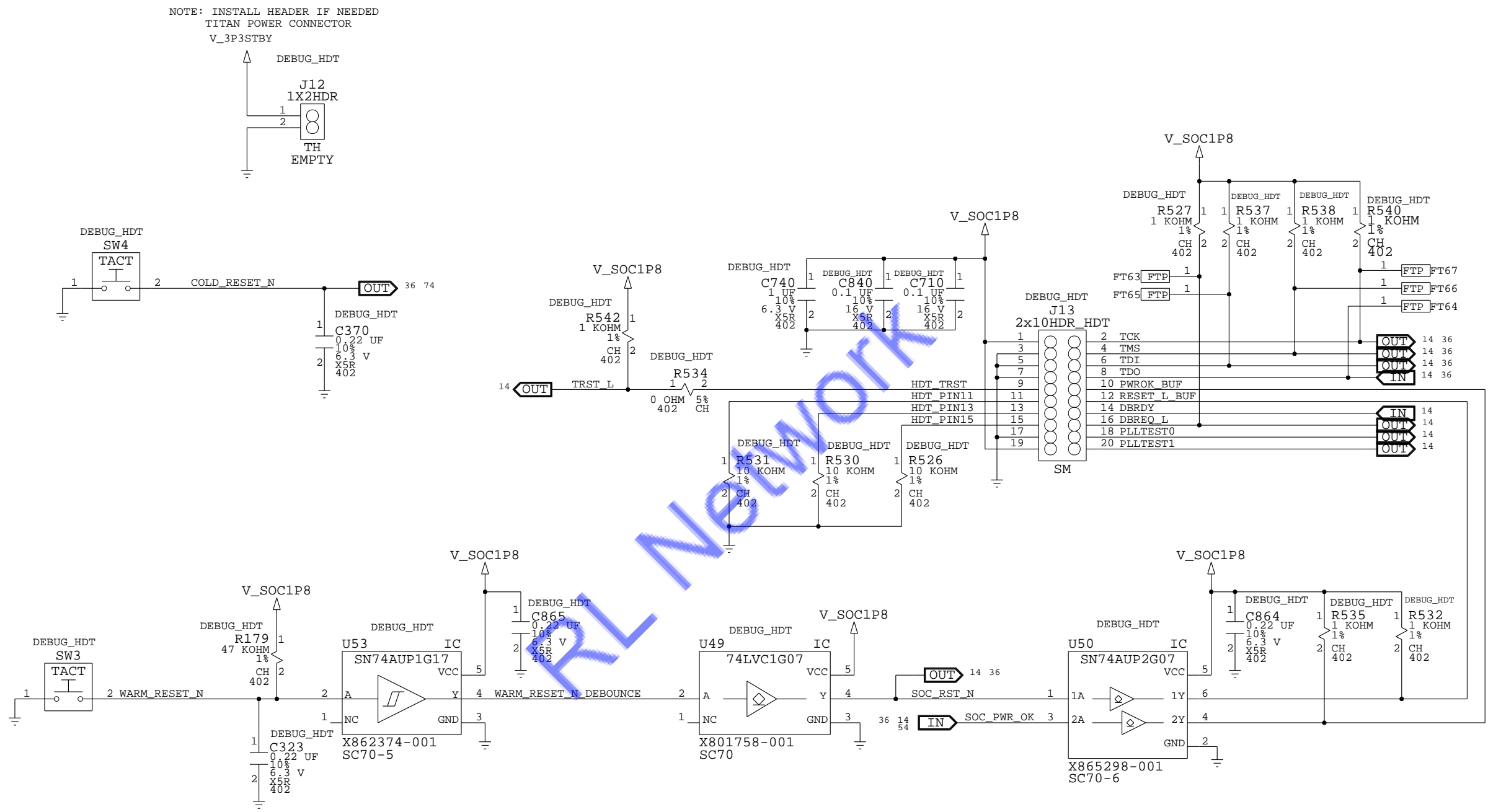


CONN: FACET BOARD

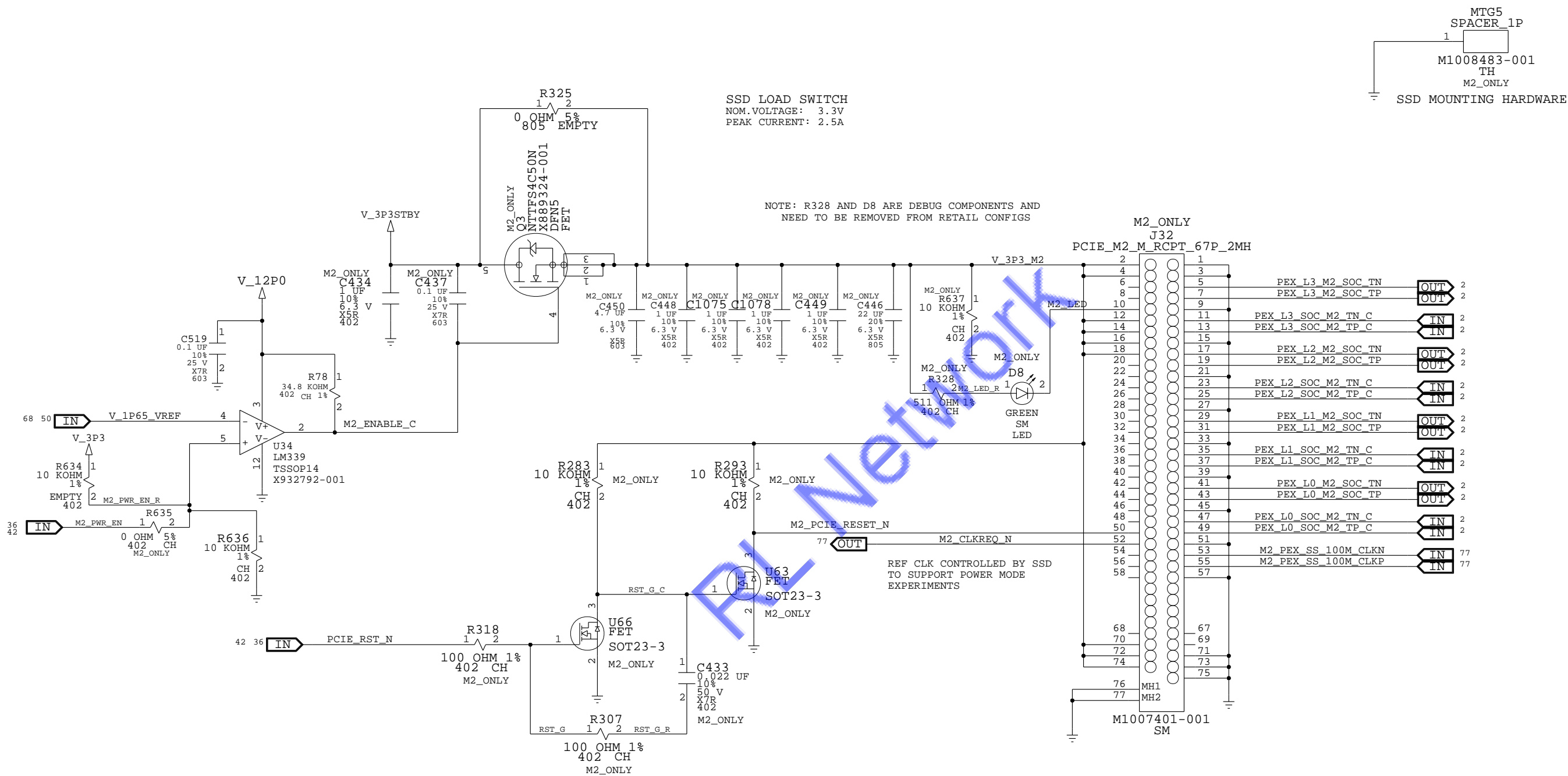


[illegible]

CONN: HDT



CONN: M.2



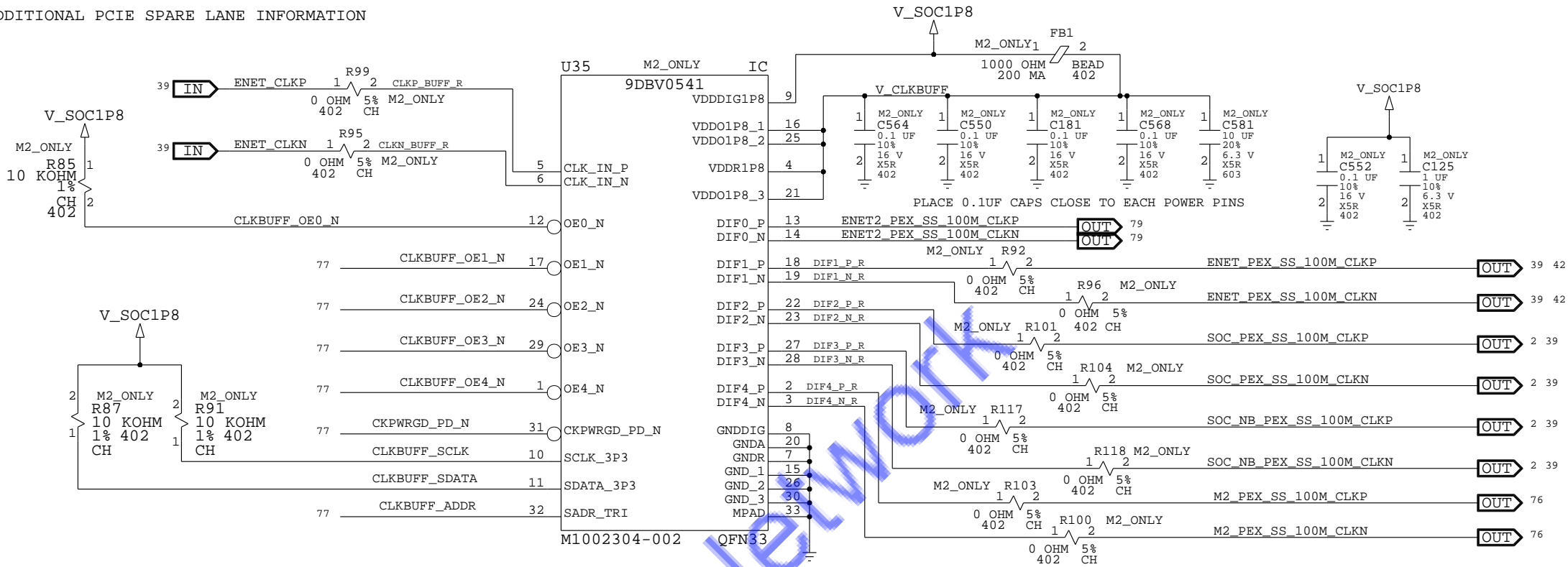
THE SSD HAS AN INTERNAL PULL-UP ON ITS PCIE RESET INPUT.  
ISOLATION OF SIGNAL PCIE\_RST\_N IS NEEDED TO ISOLATE  
SOUTHBRIDGE OUTPUT FROM SSD PULLUP



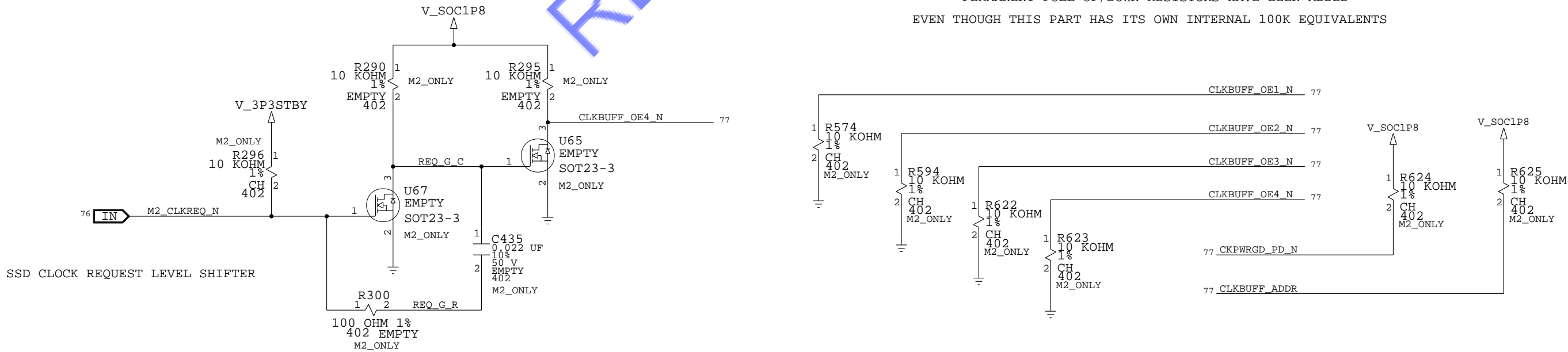
# CLOCK BUFFER

## NOTES:

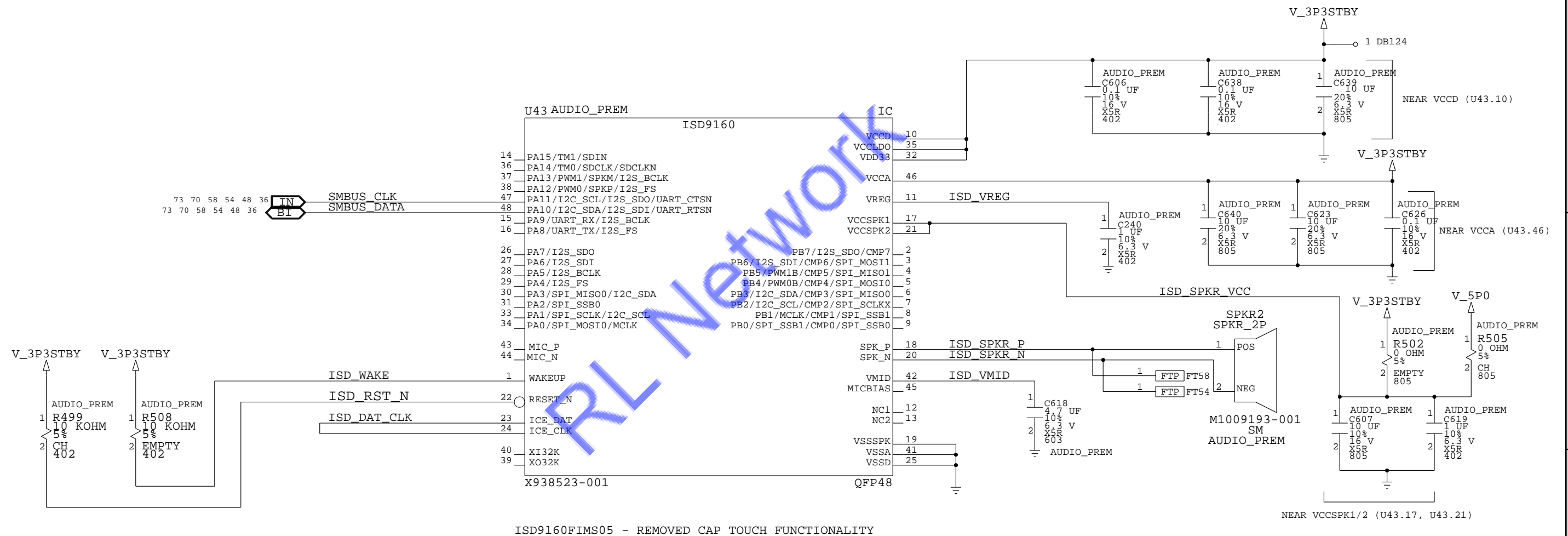
- 1.TO ENABLE ENET2 CLOCK ON J28 HEADER, UNSTUFF R85. U35 HAS INTERNAL PULL DOWN.
- 2.SEE PAGES 2 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION



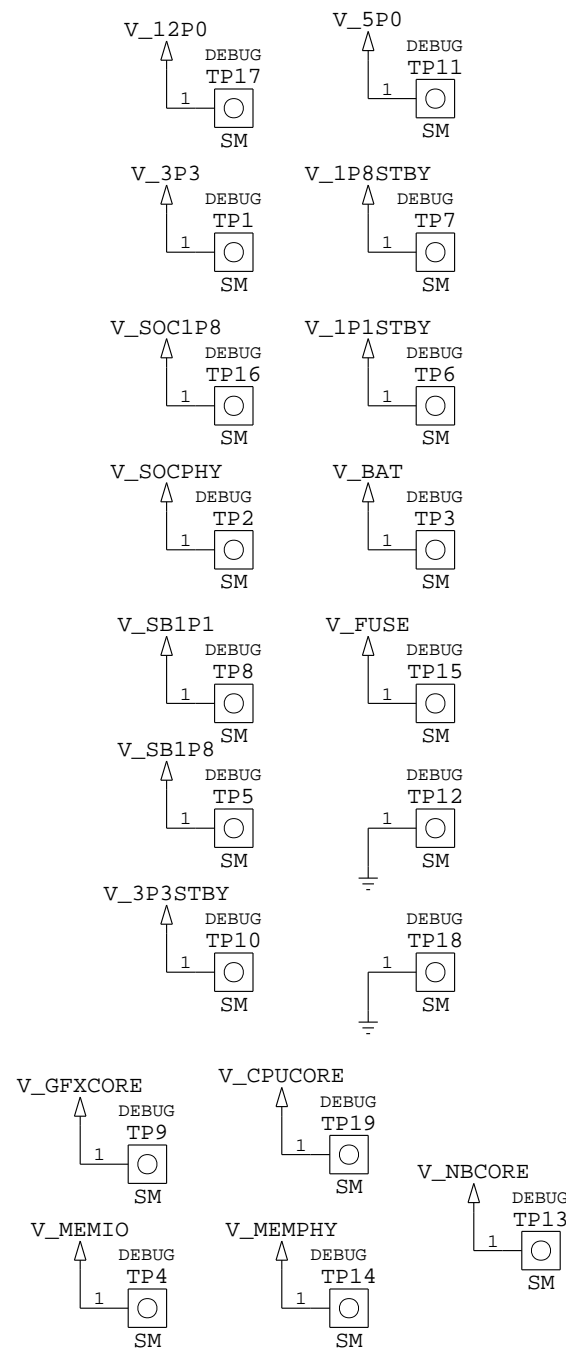
TO ADDRESS LONG TERM RELIABILITY CONCERNS  
PERMANENT PULL UP/DOWN RESISTORS HAVE BEEN ADDED  
EVEN THOUGH THIS PART HAS ITS OWN INTERNAL 100K EQUIVALENTS



## PREMIUM/SE/LE SKU ONLY

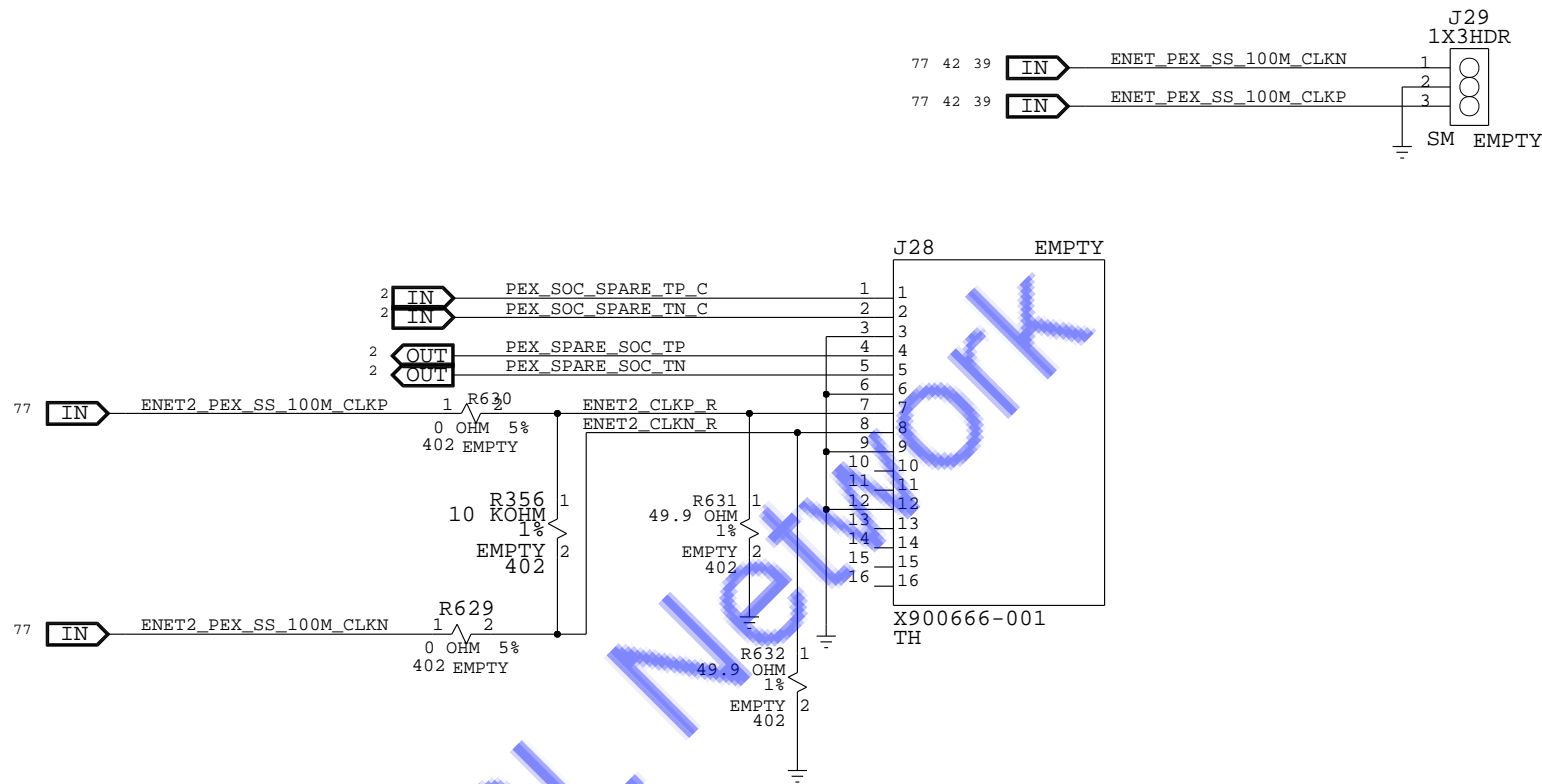


# DEBUG: VR HEADERS, TEST POINTS, CONNECTORS



NOTE: THESE TEST POINTS ARE NOT TO BE USED FOR VOLTAGE REGULATOR QUALIFICATION TEST POINTS

## PCIE CONNECTORS



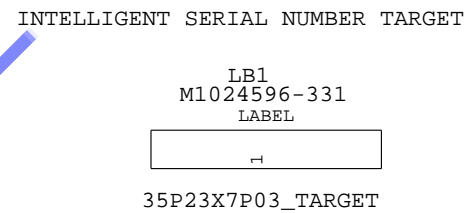
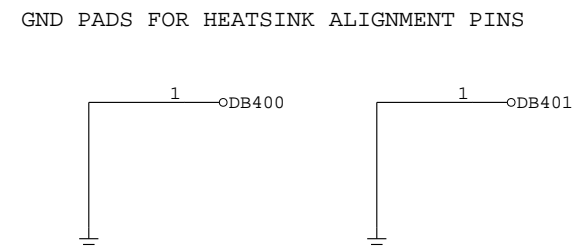
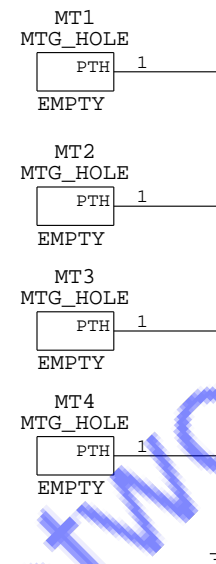
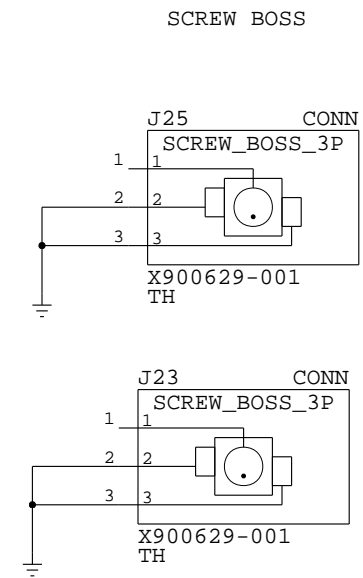
- NOTES: TO ENABLE 100 MHZ REF CLOCK ON HEADER J28:
- 1.WHEN CLOCK BUFFER U35 IS INSTALLED: POPULATE R629 AND R630.
  - 2.WITHOUT CLOCK BUFFER INSTALLED:
    - A.POPULATE R631 AND R632.
    - B.WIRE JUMPER ETHERNET 100 MHZ CLOCK FROM HEADER J29.1 AND J29.3 TO J28.8 AND J28.7 RESPECTIVELY.
  - 3.SEE PAGES 2 AND 77 FOR ADDITIONAL PCIE SPARE LANE INFORMATION.

MT3  
MTG\_HOLE  
PTH 1  
EMPTY

MT4  
MTG\_HOLE  
PTH 1  
EMPTY

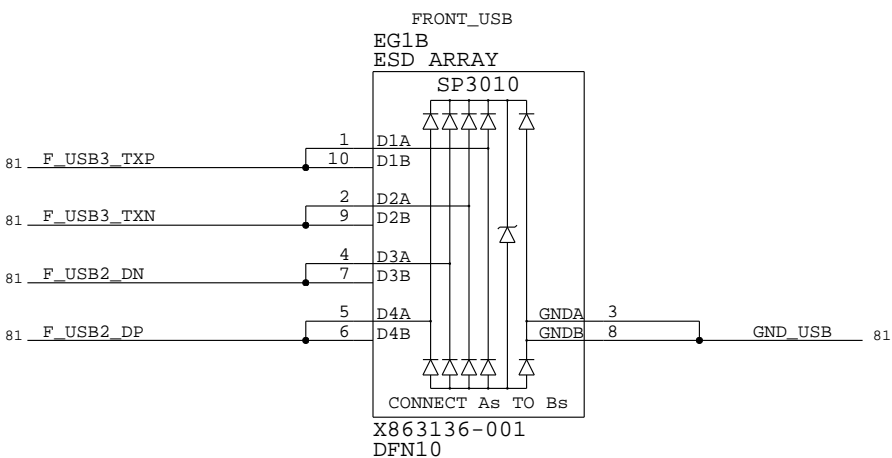
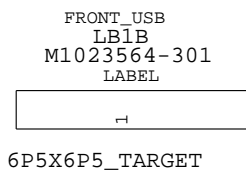
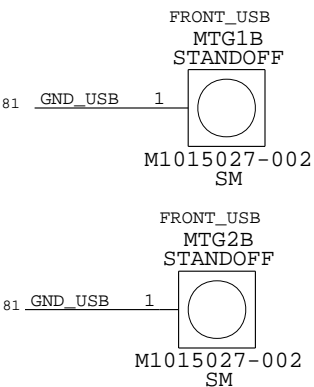
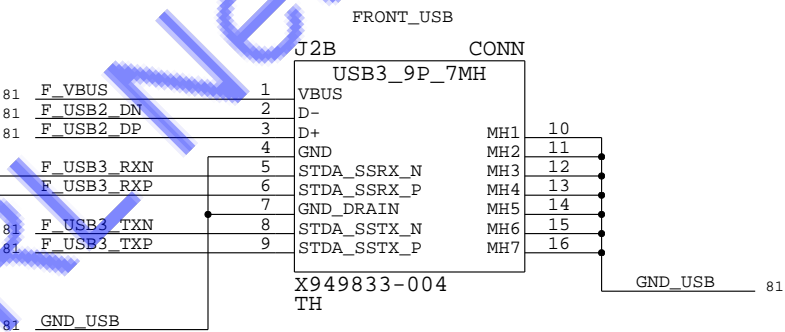
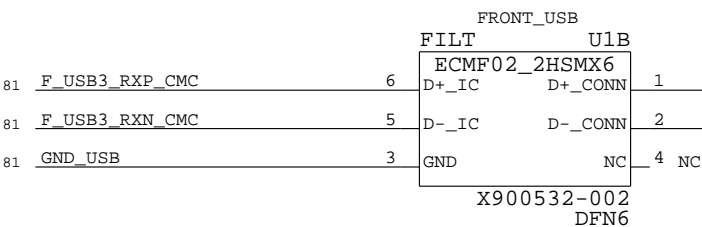
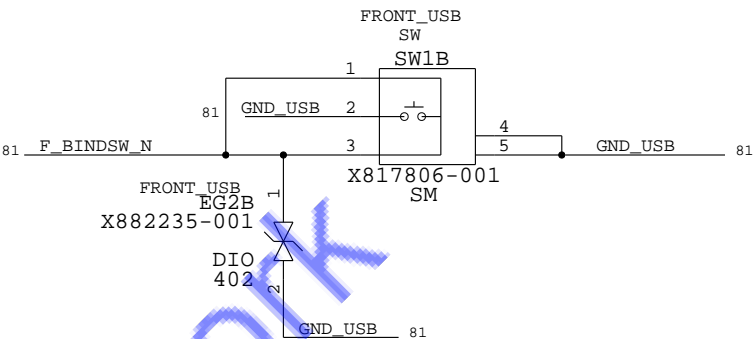
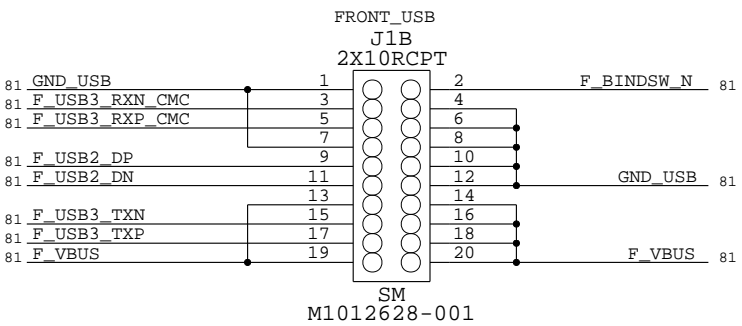
INTELLIGENT SERIAL NUMBER TARGET

LB1  
M1024596-331  
LABEL



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
NA	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,GI	PCB_GI
M1037358-002	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,OSH	PCB_OSP

# FRONT PANEL USB - NESTED PCB



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
M1033394-001	FR4	PCB1B	PCB,CACTUS,FAB E RETAIL,FRONT USB,8 LAYERS,GI	FRONT_USB

8		7		6		5		4		3		2		1		
BOM DEFINITIONS																
D	BOM		DEFINTION													D
	AUDIO		INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION													
	AUDIO_PREM		INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION													
	COMMON		ALL COMPONENTS WITH NO BOM PROPERTY													
	DEBUG		COMPONENTS REQUIRED FOR BRING UP & DEBUG													
	DEBUG_HDT		HDT-RELATED DEBUG COMPONENTS													
	DEBUG_SHUNT		COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL													
	EMMC_BASE		DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM													
	EMMC_HYNIX_16NM		HYNIX EMMC DEVICE													
	EMMC_SAMSUNG_14NM		SAMSUNG EMMC DEVICE													
C	EMMC_TOSHIBA_15NM		TOSHIBA EMMC DEVICE													C
	GDDR5_BASE		DUMMY PLACE HOLDER FOR GDDR5. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM													
	GDDR5_HYNIX		HYNIX GDDR5 MEMORY													
	GDDR5_SAMSUNG		SAMSUNG GDDR5 MEMORY													
	FRONT_USB		COMPONENTS ON THE FRONT PANEL USB													
	KIC_BASE		DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL													
	KIC_DEV		DEBUG VERSION OF KRAKEN													
	KIC_RETAIL		RETAIL VERSION OF KRAKEN													
	M2_ONLY		POPULATE TO SUPPORT AN M.2 INTERFACE													
	NO_M2		POPULATE WHEN THERE IS NO M2. INTERFACE													
B	PCB_GI		FAB TYPE: GOLD													B
	PCB_OSP		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK													
	PCB_OSP_BLACK		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK													
	RTC_RETAIL		RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS													
	RTC_XDK		RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS													
	SOC_BASE		DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM													
	SOC_EMPTY		DOES NOT STUFF ANUBIS													
	SOC_INCLUDE		STUFFS ANUBIS													
	VR_FIXED		SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM													
	VR_MM		ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED													
A																A
8		7		6		5		4		3		2		1		
												MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 82/82	CSA PAGE 82/82	VER 0.991